No. ________

IN THE
Supreme Court of the United States

LONE STAR SILICON INNOVATIONS LLC,

Petitioner,

v.

ANDREI IANCU, Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office,

Respondent.

On Petition for Writ of Certiorari to the United States Court of Appeals for the Federal Circuit

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PETITION FOR WRIT OF CERTIORARI

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QUESTIONS PRESENTED

Any person, other than the patent owner, may request initiation of inter partes review proceedings against an issued patent, by filing a petition with the Patent and Trademark Office that identifies challenged claims and the grounds asserted for each challenged claim. 35 U.S.C. §§ 311–12. The Patent Trial and Appeal Board ("PTAB" or "Board") decides whether to institute trial, based on the information in the petition and, if filed, a patent owner preliminary response. 35 U.S.C. § 314. At the conclusion of an instituted trial, the Board issues a final written decision determining the patentability of any patent claim challenged by the petitioner. 35 U.S.C. § 318. The questions presented are:

(1) whether, in inter partes review proceedings, the Board may issue a final written decision that invalidates duly issued patent claims based on a ground not asserted by the petitioner in the corresponding petition; and

(2) whether judicial review is available to remedy the Board's unauthorized final decision invalidating those claims based on a ground not asserted in the petition.

PARTIES TO THE PROCEEDING AND RELATED CASES

Lone Star Silicon Innovations LLC ("LSSI") was appellant below in proceedings before the U.S. Court of Appeals for the Federal Circuit. LSSI was the respondent/patent owner in proceedings before the PTAB.

Respondent Andrei Iancu, Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office, was an intervenor below at the Federal Circuit.

Micron Technologies, Inc. was initially an appellee below, and was petitioner before the PTAB. While the appeal was pending, the Federal Circuit granted Micron Technologies, Inc.'s unopposed motion to withdraw from further participation in the appeal, upon their settlement of the case. Pursuant to Rule 12.6, petitioner believes that Micron Technologies, Inc. has no interest in the outcome of this petition.

RULE 29.6 DISCLOSURE STATEMENT

Petitioner Lone Star Semiconductor Innovations LLC is a wholly owned subsidiary of Longhorn IP LLC, which is wholly owned by Tanit Ventures Inc. Tanit Ventures Inc. has no parent corporations and no publicly held company owns 10% or more of its stock.

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PETITION FOR WRIT OF CERTIORARI

Petitioner respectfully requests a writ of certiorari to review the judgment of the United States Court of Appeals for the Federal Circuit.

OPINIONS BELOW

The Federal Circuit's non-precedential opinion is unreported, but available at 809 F.App'x 773 and is reprinted in the Appendix to the Petition ("App.") at App. 3–18. Its non-precedential order denying rehearing en banc is unreported and is reprinted at App. 1–2.

The Final Written Decision of the Patent Trial and Appeal Board ("PTAB" or "Board") is reprinted at App. 19–71. The PTAB's decision to institute inter partes review is reprinted at App. 78–99, and its Decision denying LSSI's petition for rehearing is reprinted at App. 72–77. Each of the PTAB's decisions is unreported.

JURISDICTION

On March 19, 2020, the Chief Justice extended the deadline to file any petition for a writ of certiorari to 150 days from the date of the lower court order denying a timely petition for rehearing. The Court of Appeals denied petitioner's timely filed petition for rehearing en banc on June 12, 2020. App. 1. This Court has jurisdiction under 28 U.S.C. § 1254(1).

CONSTITUTIONAL AND STATUTORY PROVISIONS INVOLVED

Each of the statutory provisions at issue was enacted by the Leahy-Smith America Invents Act (AIA), Pub. L. No. 112-29, 125 Stat. 284 (2011), and is now codified in Title 35 of the United States Code. The

text of each relevant provision is set forth at App. 100–113.

INTRODUCTION AND STATEMENT OF THE CASE

A. AIA Trial Proceedings

In 2011, Congress passed the Leahy-Smith America Invents Act ("AIA"), which created trial proceedings before the PTAB. Pub. L. No. 112-29, 125 Stat. 284 (2011). Congress explained that "[t]he Act converts inter partes reexamination from an examinational to an adjudicative proceeding, and renames the proceeding 'inter partes review.'" H.R. REP. NO. 112-98, at 46–47 (2011).

Inter partes review is an adversarial adjudicatory process, relying upon opposing parties who advocate for and against validity of a challenged patent. Under the AIA, "[a]ny person other than the patent owner can file a petition for inter partes review." *Oil States Energy Servs., LLC v. Greene's Energy Grp., LLC*, 138 S. Ct. 1365, 1371 (2018) (citing 35 U.S.C. § 311(a) (2012 ed.)). Unlike ex parte reexamination the USPTO cannot initiate an inter partes review proceeding of its own volition. *Compare* 35 U.S.C. § 303(a) ("On his own initiative, and any time, the Director may determine whether a substantial new question of patentability is raised by patents and publications discovered by him . . .") *with SAS Inst. v. Iancu*, 138 S.Ct. 1348, 1355 (2018) (section 311(a) "doesn't authorize the Director to start proceedings on his own initiative."). Accordingly, the AIA requires the petition to identify "with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim." 35 U.S.C. § 312(a)(3); *SAS*

Inst., 138 S.Ct. at 1355–58. The patent owner has the right to oppose the petition, by filing a preliminary response that asserts "reasons why no inter partes review should be instituted." 35 U.S.C. § 313. Among exemplary reasons not to institute, the patent owner may argue that "[t]he prior art lacks a material limitation in a challenged claim," or that "[t]he prior art does not teach or suggest a combination that the petitioner is advocating." PTAB Consolidated Trial Practice Guide (Nov. 2019), *available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

To decide whether to institute trial, the Board[1] sits in judgment to preliminarily determine whether "the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). The AIA requires the promulgation of regulations "setting forth the standards for the showing of sufficient grounds to institute a review under section 314(a)." But neither the Director nor the Board has statutory authority to conduct an IPR trial of its own design, i.e., that departs from the invalidity challenges alleged in the petition. *See SAS Inst.*, 138 S.Ct. at 1355–56. Indeed, the relevant regulations limit institution to "the grounds of unpatentability asserted for each claim." 37 C.F.R. § 42.108(a).

If the Board institutes trial, the adversarial process continues, with "[m]any of the usual trappings of litigation," where the petitioner and the patent

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[1] The Director of the USPTO has designated authority under § 314 to the Board. *See* 37 C.F.R. § 42.4(a).

owner "conduct discovery and join issue in briefing and at an oral hearing." *SAS Inst.*, 138 S.Ct. at 1354. Ultimately, the Board must "issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added" by amendment. 35 U.S.C. § 318(a).

The AIA allows that "[a] party dissatisfied with the final written decision of the Patent Trial and Appeal Board under section 318(a) may appeal the decision" to the Federal Circuit. 35 U.S.C. § 319. In contrast, judicial review of the institution decision is generally unavailable. 35 U.S.C. § 314(d); *Cuozzo Speed Techs., LLC v. Lee*, 136 S.Ct. 2131, 2139 (2016). But this Court has emphasized that "nothing in § 314(d) or *Cuozzo* withdraws our power to ensure that an inter partes review proceeds in accordance with the law's demands." *SAS Inst.*, 138 S.Ct. at 1359.

B. IPR Proceedings Before the PTAB

This case began at the PTAB when Micron filed its IPR Petition on June 9, 2017, challenging claims 1, 2, 5–7, and 10 of U.S. Patent No. 6,388,330 ("the '330 patent"). JA60–128; *see* App. 4–5, 20. Micron asserted a single ground of invalidity, arguing that all of the claims are invalid for obviousness in view of a particular combination of disclosures in Watatani[2] and Tanaka[3]. JA70; *see* App. 4–5, 25.

Obviousness under 35 U.S.C. § 103 requires proof that all elements of a claimed invention are taught or suggested by the prior art and that one skilled in the

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[2] U.S. Patent No. 6,153,511 to Watatani et al.

[3] Masayuki Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47-48.

art would be motivated to combine the teachings as claimed. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). In attempting to satisfy this requirement with respect to independent claims 1 and 6, Micron argued that Watatani's first prior art embodiment, shown in Watatani's FIG. 1F, disclosed all elements but one for each claim. JA95–104; JA108–119. For the missing element, requiring "an etch stop layer of silicon nitride . . . having a dielectric constant below 5.5," Micron argued that Tanaka discloses a silicon nitride material having a dielectric constant below 5.5. JA101–103; JA113–115.

Dependent claim 2, which includes all elements of claim 1, further recites "the etch stop layer is a multilayer structure." Micron argued this further element of claim 2 was disclosed by separate structure illustrated in Watatani's FIGS. 5A–5I:

> Watatani expressly describes an etch stop layer that includes "three or more layers" of silicon nitride. Ex.1005, Watatani, 7:54-55. Such multilayer silicon nitride layers were well known in the prior art Ex.1003, Fair Decl. ¶¶105-107. Indeed, in its normal operation, the prior art Novellus Concept One CVD tool, which was widely used in the semiconductor industry long before the filing date of the 330 Patent, deposited multilayer silicon nitride films through "successive deposition." *Id.* ¶106.

JA105. As quoted above, Micron cited the separate SST 1987 article[4] to support its argument that "[s]uch

[4] Continuous Process CVD System, SOLID STATE TECHNOLOGY (Oct 1987) ("SST 1987").

multilayer structures," meaning Watatani's alleged "three or more layers" of silicon nitride, were well known. *See* JA105–106 (claim 2). Micron neither argued nor supplied any evidence showing that the "multilayer silicon nitride layers" disclosed by the SST 1987 article were used as etch stops. *See id.* Dependent claim 7, which includes all elements of claim 6, further recites "the via and channel etch stop layers are a multilayer structure." Micron argued identically that this further element of claim 7 was disclosed by Watatani's FIGS. 5A–5I. JA119–120.

In attempting to prove that one skilled in the art would have been motivated to combine these teachings, Micron asserted that secondary references would have motivated the use of Watatani's multilayer etch stop (shown in FIGS. 5A–5I) in the conventional embodiment represented by Watatani's FIG. 1F:

> Although Watatani describes the multilayer silicon nitride etch stop in the context of the embodiment of its claimed invention, a POSA would have been motivated to use Watatani's multilayer approach in any dual damascene structure, including a conventional dual damascene structure, in order to achieve the advantages that the multilayer approach provides.

JA106 (claim 2), JA121 (claim 7). Relying on the Wang patent[5] and an expert declaration, the Petition further asserted that a skilled artisan would have recognized certain benefits to using a multilayer silicon nitride etch stop. JA105–106, JA119–120. In addition, the

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[5] U.S. Patent No. 6,017,791

petition used the SST 1987 article to establish that a system for producing a multilayer film was available and that multilayer films were known to be more uniform, proffering this as evidence of a motivation to make the alleged combination with reasonable expectation of success. JA105–106, JA120–121.

LSSI filed a Preliminary Response supported by an expert declaration. JA140–207; JA1027–1107. Among other arguments, LSSI argued that dependent claims 2 and 7 are not invalid over the asserted Tanaka and Watatani references because Watatani teaches that its multi-layer etch stop requires layers of different materials and consequently fails to disclose the claimed multilayer silicon nitride etch stop structure. JA197–205.

The Board subsequently issued a Decision on Institution, expressly agreeing that Watatani does not disclose any etch stop layer formed of multiple layers of silicon nitride. App. 78–100. "[W]e are persuaded, at least at this stage of the proceeding, that Watatani does not disclose the limitations of claims 2 and 7 under a claim construction that Petitioner concedes is applicable in this proceeding." App. 96. Notwithstanding this factual finding, the Board ordered institution of trial on each of the challenged claims, including dependent claims 2 and 7. App. 99.

To justify institution, the Board invoked a distinct theory of obviousness. Under the Board's theory, Watatani's multilayer etch stop—formed of multiple non-silicon nitride layers—is ignored in favor of the allegedly general knowledge that multiple thin silicon nitride layers could be produced and would yield more uniform films. App. 96–98.

LSSI filed a Request for Rehearing seeking reconsideration of the Board's decision on claims 2 and 7 because the Board had instituted trial on a ground of invalidity not asserted in Micron's petition. JA240–255; App. 72–76. The Board denied the request, asserting that the Decision on Institution was not based on a new ground because the SST 1987 article was used as evidence of the knowledge of a skilled artisan. App. 75. In its subsequent patent owner response, LSSI maintained that the Board lacked authority to consider any ground not asserted in Micron's petition. App. 7. Micron filed a reply supported in part by a newly cited Yota[6] article, and LSSI filed a sur-reply to address Micron's new evidence. App. 7–8.

The Board entered a Final Written Decision, concluding that all challenged claims were unpatentable, including dependent claims 2 and 7. App. 19–71. While the Board continued to characterize its rationale as based on the combination of Watatani and Tanaka, its reasoning ignored Watatani and substituted SST 1987, Wang, and Yota into the combination—explicitly replacing Watatani's etch stop structures. App. 58–59.

C. The Federal Circuit Appeal

LSSI appealed to the Federal Circuit from the Board's final written decision. The Federal Circuit upheld the Board's rulings invalidating all challenged claims, including claims 2 and 7 of the '330 patent. App. 5. The Federal Circuit held that LSSI's appeal

[6] Jiro Yota et al., Comparison between HDP CVD and PECVD Silicon Nitride for Advanced Interconnect Applications, PROC. OF THE IEEE 2000 INT'L INTERCONNECT TECH. CONFERENCE, 76–78 (IEEE Electron Devices Soc'y, 2000).

was barred by 35 U.S.C. § 314(d). App. 10. The court reasoned that LSSI's challenge was "'closely tied' to the Board's 'decision to initiate inter partes review.'" App. 13.

The Federal Circuit further held that the Board was not "obliged to 'ignore the skilled artisan's knowledge when determining whether it would have been obvious to modify the prior art.'" App. 11. The court held that the instituted ground, like the petition, was based on Watatani in view of Tanaka, and that "additional references were being relied on exclusively for their teachings about what was well-known in the art." App. 12.

LSSI filed a petition for rehearing or rehearing en banc, which the Federal Circuit denied in a per curium decision with no further reasoning. App. 1–2.

REASONS FOR GRANTING THE PETITION

I. THE DECISION BELOW PRESENTS ISSUES OF EXCEPTIONAL IMPORTANCE

When expansively applied, the "no appeal" rule in 35 U.S.C. § 314(d) deprives aggrieved parties of their right to appeal from final PTAB decisions that were wrongly decided. This case is an example, because the Federal Circuit broadly and erroneously interpreted § 314(d) by conflating review of the final PTAB decision with review of the institution decision.

Although this Court has attempted to balance the need for judicial review against the need for efficiency, *see Cuozzo*, 136 S.Ct. at 2139–40, the effect of related statutory language remains uncertain. Emphasizing the "strong presumption" in favor of reviewability, *SAS Institute* reasoned "*Cuozzo* concluded that § 314(d) precludes judicial review only of the director's

'initial determination' under § 314(a) that 'there is a reasonable likelihood that the claims are unpatentable on the grounds asserted.'" 138 S.Ct. 1359. *SAS Institute* therefore held that the Director had exceeded his statutory authority, under 35 U.S.C. § 318, by limiting the inter partes review to fewer than all of the claims that had been challenged. *Id.*

Subsequently, this Court clarified that § 314(d) "indicates that a party generally cannot contend on appeal that the agency should have refused 'to institute an inter partes review.'" *Thryv Inc. v. Click-To-Call Techs. LP*, 140 S.Ct. 1367, 1373 (2009). *Thryv* ultimately concluded that the time bar under § 315(b) "is integral, indeed a condition on, institution," which therefore precludes review on appeal because "§ 315(b) governs institution and nothing more." *Id.* But *Thryv* distinguished *SAS Institute*, because appeals springing from § 318(a) based on "the manner in which the agency's review 'proceeds' once instituted" are reviewable, in contrast to appeals questioning "whether the agency should have instituted review at all." 140 S.Ct., at 1376.

Following *Thryv*, the Federal Circuit held that § 314(d) does not preclude review of the Director's discretion to join a follow-on petition filed by the same PTAB petitioner "as a party" under § 315(c). *Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1332 (Fed. Cir. 2020). There, the Federal Circuit distinguished *Thryv*, reasoning that "Windy City's cross-appeal does not challenge the Board's decision to institute Facebook's follow-on petitions, but challenges whether the Board's joinder decisions exceeded the statutory authority provided by § 315(c)." *Id.*

On other issues, the Federal Circuit's application of *Thryv* has significantly expanded the Board's discretion by expanding the scope of § 314(d). The Federal Circuit has held that § 314(d) precludes review of the Board's real party-in-interest determinations under 35 U.S.C. § 312(a)(2). *ESIP Series 2, LLC v. Puzhen Life USA, LLC*, 958 F.3d 1378, 1386 (Fed. Cir. 2020); *Fall Line Patents, LLC v. Unified Patents, LLC*, 818 F.App'x 1014, 1017–18 (Fed. Cir. July 28, 2020) (further holding that mandamus review is unavailable to address real party-in-interest determinations). The Federal Circuit has also held that the Board's acceptance of a "tardy" petition and request for joinder, at the institution phase, is not reviewable on appeal. *Fitbit, Inc. v. Valencel, Inc.*, 964 F.3d 1112, 1115 (Fed. Cir. 2020).

The bounds of the no-appeal rule under § 314(d) remains a hotly litigated issue, and the Court's further guidance through this case would serve to define the issue and provide certainty below.

A. Constraining the Board's Final Written Decision to Its Statutory Authority Is Critical to the Efficient Operation of AIA Trials and the Patent System

1. Appellate review protects the policies enacted by Congress. AIA trials are supposed to provide a streamlined process by relying on the petition to define the scope of the trial. To initiate trial proceedings, the AIA requires a petitioner to identify grounds of invalidity, including evidence and arguments. *See* 35 U.S.C. § 311 (petitioner initiates IPR). Specifically, the petition must identify "with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the

evidence that supports the grounds for the challenge to each claim." 35 U.S.C. § 312(a). Inter partes review proceeds in an expedited fashion, by design, which places the "utmost importance" on identifying the evidence that supports the ground "with particularity." *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (quoting 35 U.S.C. § 312(a)(3)). When deciding whether to initiate a trial, the Board weighs the grounds in view of contrary evidence and arguments marshalled by the patent owner. *See* 35 U.S.C. § 318(a).

Accordingly, the AIA requires the petition to identify the asserted grounds of invalidity "with particularity," such that the patent owner can adequately respond through the limited briefing afforded by the procedure. *See* 35 U.S.C. § 312(a)(3). Contrary to the framework outlined in the AIA, allowing the Board to inject new issues or modify the asserted grounds prejudices the patent owner by obligating the patent owner to dispute issues that the petitioner never raised and as to which the Board is an advocate rather than a neutral decision maker.

The AIA contemplates the patent owner response as "a response to the *petition* . . . after an inter partes review has been instituted. 35 U.S.C. § 316(a)(8) (emphasis added). The USPTO's regulations and trial practice guide similarly allow the patent owner to file "a response to the *petition*," further explaining that the "patent owner response is filed as an opposition." 37 C.F.R. § 42.120 (emphasis added); *see* PTAB Consolidated Trial Practice Guide, at 64–65. The USPTO regulations allow a reply, which "may only respond to arguments raised in the corresponding

opposition, patent owner preliminary response, or patent owner response." 37 C.F.R. § 42.23(b).

This process can efficiently hone the disputed issues only if the rules are stringently followed. If the petitioner's reply asserts new evidence and arguments in support of the grounds asserted in the petition (such as additional evidence demonstrating the knowledge of one skilled in the art or of motivation to combine teachings in the prior art in the manner alleged), this new information can now be addressed through a patent owner sur-reply. *See* PTAB Consolidated Trial Practice Guide, at 73–74.

In contrast, if the grounds of invalidity are permitted to change during the proceeding, the patent owner faces extreme prejudice. The petitioner's reply brief then becomes a tool of ambush, an opportunity to interject new legal argument and evidence in support of the new alternative ground after the patent owner has filed its response and deposed petitioner's expert. A patent owner sur-reply is an inefficient and inadequate remedy in this situation. In short, when the Board introduces or otherwise permits new grounds into the proceedings, it subverts the efficient course of briefing that was core to the design of AIA trials.

Congress recognized the need for separate ex parte and inter partes procedures for reconsidering issued patents. Ex parte reexamination provides a separate mechanism by which the USPTO can reconsider an issued patent. The Director can, sua sponte, raise issues for ex parte reexamination. 35 U.S.C. § 303(a). Once initiated, the reexamination is inquisitorial, allowing USPTO examiners to weigh the art and refine their rejections. But ex parte reexamination includes procedural protections that prevent an

overzealous examiner or PTAB panel from steamrolling the patent owner. In appeals to the PTAB during these proceedings, when the PTAB formulates a new ground of rejection, at the applicant's request the issue returns to the examiner who will hear a fresh, unconstrained response from the patent owner. USPTO Manual Patent Examination and Procedure § 1214.01, *available at* https://mpep.uspto.gov/RDMS/MPEP/e8r9#/e8r9/d0e128986.html. This provides the patent owner with a symmetric opportunity to address the new ground and marshal additional evidence or argument in response. *Id.*

In contrast to ex parte procedures, AIA trials are designed to be speedy, efficient, and adversarial. The PTAB subverts Congressional intent by introducing or otherwise allowing new grounds in the proceedings. Such changes substantially affect the balance of efficiency and fairness outlined by Congress in the America Invents Act.

Moreover, by pursuing separate invalidity theories of its own making, the Board risks becoming improperly vested in a negative outcome for patent owners. Even the appearance of bias undercuts the legitimacy of the PTAB.

Appellate review and prohibition of new grounds is the only way to ensure that the scope of AIA trial proceedings stay within the prescribed scope (i.e., that set forth in the petition) and the only way of guaranteeing that the PTAB remains a neutral arbiter of the specific invalidity issues raised by the petitioner.

2. The Federal Circuit is capable of reviewing and remedying board decisions that are based on improper

grounds, despite its lament that LSSI's requested relief would require the court to compare the Board's institution decision "to the particular language used in Micron's petition." App. 13. First, the Federal Circuit's analysis applies to whether the Board's final decision adhered to the initial petition, not the Board's institution decision. Second, such analysis is typical for the Federal Circuit on other issues.

Identifying when a final decision exceeds the Board's authority by relying on new grounds is precisely within the ability of a reviewing court. The limits imposed by the Administrative Procedure Act ("APA"), requiring notice and opportunity to respond to new grounds, are analogous even though they do not control here. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1335–36 (Fed. Cir. 2020) (nullifying improperly raised third ground identified in the Board's institution decision despite notice and opportunity to respond to the new ground). Although the APA serves different purposes than the structured procedure defined by the AIA, improperly decided cases must be unwound under either statute to give effect to the Congress's duly enacted laws. Comparing the grounds relied upon by the Board to invalidate claims to those asserted in a petition does not require expertise beyond the ken of the Federal Circuit. That court regularly evaluates the scope of grounds asserted by examiners and the Board during prosecution, and by petitioners and the Board during IPR and other post-grant proceedings. *See, e.g.*, *Koninklijke Philips*, 948 F.3d at 1335–36; *In re IPR Licensing, Inc.*, 942 F.3d 1363, 1369–70 (Fed. Cir. 2019); *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1377–78 (Fed. Cir. 2016); *In re NuVasive, Inc.*, 841 F.3d 966, 971 (Fed. Cir. 2016).

In the absence of judicial review, fairness to patent owners in these streamlined IPR proceedings cannot be assured. The Court's precedents above, and the assurances of procedural due process simply do not provide adequate protection. This is especially true if the rules of institution allow the Board to become an advocate for the Petitioner.

3. The Federal Circuit's decision in this case evinces a conflict within its own precedent.

Separately, the Federal Circuit has held that the Board lacks authority to invalidate on grounds that are not presented in a petition for inter partes review. *Koninklijke Philips*, 948 F.3d at 1335. In the case below, the panel disregarded this binding precedent, holding instead that such an issue is not appealable. App. 10.

In *Koninklijke Philips*, the petition presented two grounds of unpatentability: (1) anticipation by the SMIL 1.0 reference, and (2) obviousness over SMIL 1.0 and the general knowledge of the skilled artisan regarding distributed multimedia presentation systems. 948 F.3d at 1333–34. The petition cited Hua and an expert declaration as evidence that a "pipelining" technique for dividing a media presentation into multiple segments was well-known and that the skilled artisan would have been motivated to use pipelining with the software disclosed in SMIL 1.0. *Id.* at 1334. The Board instituted review on both grounds raised by Google, as well as on an additional third ground: "obvious[ness] over SMIL 1.0 and Hua based on the arguments and evidence presented in the Petition." *Id.* With respect to the third ground, the Federal Circuit held that the Board "erred by instituting inter partes review based on a combination of prior art references not advanced

in Google's petition." *Id.* at 1335. This result followed despite the third ground being based on the same references cited in the petition.

The decision below is also inconsistent with the *Cuozzo* and *SAS Institute* decisions and is not required by *Thryv*. Each of those cases allows for appellate review of the Board's conduct of trial proceedings and its resulting patentability determinations under the longstanding policy favoring judicial review of final administrative actions. In *SAS Institute*, this Court observed that "[f]rom the outset, we see that Congress chose to structure a process in which it's the petitioner, not the Director, who gets to define the contours of the proceeding." *SAS Institute*, 138 S.Ct. at 1355. The Federal Circuit must have the ability to enforce this clear directive by ensuring that PTAB final decisions stay within this limited scope.

Review after a final written decision carries significantly different policy concerns, compared to direct appeal from an institution decision. The Federal Circuit has observed this difference, for example, in *Magnum Oil*, where it found that the Board erred in making a new obviousness argument on behalf of the petitioner despite the USPTO's protest that the new theory "could have been included in a properly-drafted petition." 829 F.3d at 1380–81 (the PTO's "authority is not so broad that it allows the PTO to raise, address, and decide unpatentability theories never presented by the petitioner."). Nothing in either 35 U.S.C. § 314(d) or *Cuozzo* prevents appellate review of aspects of a Board's final decision "merely because its final analysis relies on statements made when it initially considered the petition." *Id.* at 1374 (distinguishing *Cuozzo*). This is exactly the

review power the Federal Circuit now discards in its decision below.

Likewise, the Federal Circuit has reviewed a PTAB petitioner's assertion that the Board improperly limited the scope of proceedings by construing the grounds asserted in the petition too narrowly. *See Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330–31 (Fed. Cir. 2019) ("the Board did not abuse its discretion by holding HPC to the obviousness theory in its petition").

In short, by conflating review of the institution decision and final decision, the Federal Circuit abrogates the responsibility it has previously claimed to oversee the PTAB's substantive review process.

B. The Scope of the Board's Authority to Decide Inter Partes Review Is One of Several Means Critical to Protecting Judicial Resources

Recognizing that the extensive process afforded in a civil action does not suit the needs of every patent dispute, Congress enacted the AIA to provide a "quick and cost effective alternativ[e] to litigation." H.R. REP. NO. 112-98, at 48; *see also* S. REP. No. 110-259, at 20 (2008) (Inter partes review is "a quick, inexpensive, and reliable alternative to district court litigation").

Access to inter partes review, however, is not without tradeoffs designed to protect judicial resources—both at the PTAB and in the district courts. Filing a PTAB petition may cause the USPTO Director to stay, transfer, consolidate, or terminate co-pending ex parte reexaminations, reissues, and derivation proceedings at the USPTO. 35 U.S.C. § 315(d). If the PTAB issues a final written decision, estoppel attaches to the PTAB petitioner or the real

party in interest or privy of the petitioner, preventing them from challenging the patent at the USPTO or in a civil action. 35 U.S.C. § 315(e). Further, even a meritorious petition is subject to denial at the discretion of the USPTO Director. *See* 35 U.S.C. § 314(a).

To further protect judicial resources, the statutory framework of the AIA limited the Board's authority to institute and maintain inter partes review. "An inter partes review may not be instituted if, before the date on which the petition for such a review is filed, the petitioner or real party in interest filed a civil action challenging the validity of a claim of the patent." 35 U.S.C. § 315(a)(1). Civil actions are automatically stayed if filed by a PTAB petitioner or real party in interest after they filed a PTAB petition. 35 U.S.C. § 315(a)(2). And PTAB petitioners are given a limited period of time for initiating inter partes review. 35 U.S.C. § 315(b). In the context of these safeguards, allowing the Board to adopt grounds not asserted in the petition risks upsetting the judicial efficiencies that Congress intentionally built into inter partes review at the PTAB.

Further, accused infringers are not without recourse where the scope of inter partes review is limited to the invalidity grounds articulated within the four corners of the petition. The petitioner has broad latitude to select the grounds to assert and to develop those grounds in its petition. Every invalidity theory is available to the accused infringer as a defense in a civil action where inter partes review is denied because of an inadequate petition.

And if the accused infringer needs time to develop its invalidity theories, district court civil actions afford the opportunity. Early in the lawsuit, the

parties exchange contention interrogatories or local patent rule disclosures. *See* Fed. R. Civ. Proc. 33(a)(2); *see*, *e.g.*, N.D.Cal. Patent L.R. 3-3, *available at* https://cand.uscourts.gov/wp-content/uploads/local-rules/patent-local-rules/Patent_Local_Rules_11-2020.pdf. Many district courts conduct a *Markman* hearing and rule on claim construction issues. *See*, *e.g.*, N.D.Cal. Patent L.R. 4-1 *et seq*. The parties typically exchange expert reports evaluating patent validity. *See* Fed. R. Civ. Proc. 26(a)(2)(B). Subsequently, the parties brief motions for summary judgment (Fed. R. Civ. Proc. 56), conduct trial before a judge or jury (Fed. R. Civ. Proc. 39), and brief motions for judgment as matter of law (Fed. R. Civ. Proc. 50). At each step, the parties refine their theories and narrow the corresponding disputed facts.

Moreover, in a case where an accused infringer loses an inter partes review trial, other defenses are available in a civil action, for example, invalidity based on prior use, patent eligibility, indefiniteness, among others. Lastly, an accused infringer knows the trade-offs between pursuing invalidity defenses in an inter partes review as opposed to during the course of a civil action. Losing a defense in a civil action because of a poorly constructed inter partes review theory is simply one such risk assumed by the accused infringer in filing an inter partes review petition.

The PTAB threatens this delicate balance of trade-offs when it modifies the theories introduced by petitioners and then invalidates claims under the modified theories in a final decision. By deciding that it cannot review such shifts of theory in final decisions, the Federal Circuit emboldens the PTAB to engage in this unauthorized practice and eliminates

the necessary means for protecting the balance enacted by Congress.

II. THE DECISION BELOW IS INCORRECT

The Federal Circuit incorrectly upheld the Board's final written decision by misapprehending this Court's precedent regarding the scope of the "no appeal" rule in § 314(d), and by misconstruing the Board's analysis of invalidity.

A. The "No Appeal" Rule In § 314(d) Does Not Preclude Review of the Grounds Relied Upon in the Final Written Decision

The panel decision incorrectly characterized LSSI's appeal as a challenge to the grounds asserted in the Board's institution decision and therefor concluded that § 314(d) prevents appellate review of the Board's grounds. App. 10. But this case appeals the Board's final decision, just like *Koninklijke Philips*, where the Federal Circuit reviewed a final decision from the Board and held "the Board erred by instituting inter partes review based on a combination of prior art references not advanced in [the] petition." 948 F.3d at 1335.

SAS Institute emphasizes that the "no appeal" clause in 35 U.S.C. §314(d) only makes the Board's decision whether to institute inter parties review non-appealable. 138 S. Ct. at 1359. LSSI's appeal did not challenge the Board's decision to institute the IPR or even its final determination invaliding independent claims 1 and 6. Instead, LSSI challenges the Board's authority to invalidate the narrower dependent claims 2 and 7 based on an invalidity theory that deviated in critical respects from the single ground alleged in the petition. In *SAS Institute*, this Court reviewed the Board's final written decision and held

that courts have authority to review the scope of IPR trial proceedings. *Id.* ("nothing in §314(d) or *Cuozzo* withdraws our power to ensure that an inter partes review proceeds in accordance with the law's demands."). *SAS Institute* therefore mandates appellate review in cases such as this one, where the Board has exceeded its statutory authority after institution.

In contrast, *Cuozzo* addresses the Board's authority to institute trial. *See SAS Institute*, 138 S.Ct. at 1359. *SAS Institute* distinguished challenges to the scope of the proceedings from "the Director's conclusion that [petitioner] showed a 'reasonable likelihood' of success sufficient to warrant 'institut[ing] an inter partes review.'" *Id.* In *Thryv*, decided after the Federal Circuit's decision here, the Supreme Court noted that *SAS Institute* remains governing law, including its holding that the judicial review is available "to ensure that an inter partes review proceeds in accordance with the law's demands" once instituted. 140 S.Ct., at 1376. In contrast, under *Thryv*, the Board's time bar decisions are not appealable because such an appeal "challenges not the manner in which the agency's review 'proceeds' once instituted, but whether the agency should have instituted review at all." *Id.*

B. Modifying the Combination of Teachings Used to Establish the Existence of the Claimed Elements in the Prior Art Constitutes a New Ground

The Federal Circuit failed to recognize that modifying the combination of teachings used to establish the existence of the claimed elements in the prior art constitutes a new ground.

1. Micron's PTAB petition asserted a single ground of invalidity against claims 2 and 7. Independent claims 1 and 6 each recite one or more "etch stop layer of silicon nitride . . . having a dielectric constant below 5.5." JA56 (6:62–64), JA57 (7:23–8:6). With respect to independent claims 1 and 6, the petition alleged the claimed etch stop layer was the "etching stopper film 12" and "etching stopper film 16" in Watatani's FIG. 1F. JA101–103 (claim 1), JA113–118 (claim 6); *see* App. 35–36. According to the Petition, the skilled artisan would have used Tanaka's low dielectric constant silicon nitride material to replace Watatani's silicon nitride etch stop layers 12 and 16. JA101–103, JA113–118; *see* App. 39.

Dependent claims 2 and 7 further recite "the etch stop layer is a multilayer structure" (JA57 (7:3–4) (claim 2)) and "the via and channel etch stop layers are a multilayer structure" (JA57 (8:12–13) (claim 7)). App. 54. But Watatani's FIG. 1F embodiment utilizes a single layer of silicon nitride to form etch stop layer 12 below channel and via dielectric layers. JA760 (FIG. 1F); *see* App. 54. The petition thus asserted that the multilayer etch stop 81 shown in Watatani's separate FIG. 5 embodiment discloses the claimed etch stop structure formed of multiple silicon nitride layers. JA105, JA120; *see* App. 54.

Micron's petition did not enumerate or describe any alternate ground that attempted to demonstrate the existence of the claimed multilayer etch stop structure based on the general knowledge of those skilled in the art. JA70, JA105–107, JA119–121. Indeed, none of the other references cited in Micron's petition disclose an etch stop structure having a multilayer construction, let alone such an etch stop formed of multiple silicon nitride layers.

The SST 1987 article does not disclose etch stop layers and was only cited to establish that equipment was available to form multilayer films of the same material. JA86, JA105–106, JA120–121 (citing JA708–709). Micron's petition never characterized SST 1987 as disclosing an etch stop of silicon nitride having a multilayer structure. The petition (JA105–106, JA120–121), supporting expert declaration (JA708–709), and reply (JA376) all carefully characterized SST 1987 as disclosing nothing more than a multilayer structure—not an etch stop. Micron never asserted that the person skilled in the art would have been motivated to apply the silicon nitride layers disclosed by SST 1987 as an etch stop, as required by law. *See KSR*, 550 U.S. at 406.

Micron's petition cited Wang only to establish knowledge that multilayer silicon nitride films have fewer pinoles. JA106, JA121 (citing JA709–710). LSSI demonstrated that Wang's process does not disclose a multilayer etch stop (JA338), petitioner did not rebut this point (*see* JA376–382), and the Board ultimately noted "Wang does not relate to etch stop layers" App. 59.

The Board recognized that Micron had mischaracterized Watatani's disclosure. In its institution decision the Board found Watatani's etch stop structure 81 is not comprised of multiple layers of silicon nitride App. 95–96, and the Board did not deviate from this finding in its final written decision App. 55-56, 58 fn. 19, 62 fn. 20. As a result, Micron's sole ground of invalidity was doomed because the combination of elements alleged would not have led to the claimed structure. The Micron petition's related assertions that a skilled artisan "would have been motivated to use Watatani's multilayer approach in

any dual damascene structure," supported by the motivation evidence allegedly supplied by SST 1987 and Wang, JA106–107; JA120–121, were rendered nonsensical and moot given that Watatani's multilayer approach requires multiple layers of different material. *See Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1164 (Fed. Cir. 2006) (proper obviousness analysis requires showing all elements of the claimed invention are found in the art before addressing motivation to combine and reasonable expectation of success). In sum, the Board's final written decision obliterated the sole ground of invalidity asserted in Micron's petition, which should have ended the inquiry.

2. The Board improperly replaced a primary reference cited in the petition with a new reference identified for the first time in petitioner's reply brief. The Federal Circuit incorrectly concluded that the instituted ground, like the petition, was based on Watatani in view of Tanaka, and that "additional references were being relied on exclusively for their teachings about what was well-known in the art." App. 11 – 12. The panel reasoned that the Board had interpreted the petition as asserting that multilayer silicon nitride layers were known in the prior art. *Id.* But the claims do not recite multilayer silicon nitride layers generally; they recite a multilayer silicon nitride structure used as an etch stop layer at a specific location of the device. Micron's petition relied exclusively on Watatani's FIG. 5 embodiment to allege that such a structure was known in art. However, the Board found that Watatani's FIG. 5 embodiment requires an etch stop formed of multiple layers of different materials and thus does not disclose an etch

stop layer formed of multiple silicon nitride layers. App. 95–96.

Rather than requiring the petitioner to carry its burden of proof based on the faulty ground alleged, the Board permitted the petitioner to reconfigure its theory, and ultimately accepted a new combination that relied on Yota, a reference asserted for the first time in the petitioner's reply, to show that it was known to use multilayer silicon nitride etch stops in damascene structures. App. 58–59. (citing petitioner's Sur-Sur-Reply [JA426]; Ex. 1017 (reply declaration) ¶ 33 [JA892]; and Ex. 1023 (Yota) [JA995–996]).

The new ground starts with the conventional damascene structure of Watatani's FIG. 1F, ignores Watatani's further teaching in FIG. 5 that multilayer etch stop layers should be formed of different materials, and ultimately relies on Yota and expert testimony first submitted with the reply as evidence that the POSA supposedly would have replaced the single layer silicon nitride etch stop layers of Watatani's FIG. 1F with multiple layers of silicon nitride.

Because its final decision relied on a ground that abandons the multilayer etch stop structure 81 of Watatani's FIG. 5 device, the Board concluded "it is unnecessary to address Petitioner's contention that Watatani discloses an etch stop layer that includes three or more layers of silicon nitride." App. 59, fn. 19. This fundamentally altered the obviousness analysis that was asserted in the petition, as the Board acknowledged:

> Because we do not rely on Watatani to teach a multilayer silicon nitride etch stop layer, we do not need to address

> Patent Owner's argument that this feature is not disclosed by Watatani (PO Resp. 54–56) or Patent Owner's related arguments regarding lack of motivation (id. at 61, 63) and defeating the purpose of Watatani's structure (id. at 67–68).

App. 63, fn. 20.

The panel decision misconstrued the petition to the extent it concluded that the petition alternatively relied on anything other than Watatani's FIG. 5 embodiment to allege it was known to use an etch stop formed of multiple silicon nitride layers. The Federal Circuit's decision quotes the Board's final decision for the petition's statement "that 'multilayer silicon nitride layers were well known in the prior art.'" App. 12. This quote plainly fails to establish that Micron's petition alleged or supplied evidence that it was known to use multilayer silicon nitride structures as etch stops in the circuit devices relevant to claims 2 and 7.

As discussed above, the Petition did not disclose or develop a separate ground of unpatentability based on SST 1987 or Wang, but without the multilayer etch stop structure 81 of Watatani's FIG. 5 embodiment. Nor does the Petition separately analyze motivations to combine the teachings of the SST 1987 article or the Wang patent directly with either Watatani's conventional FIG. 1F embodiment or Tanaka's silicon nitride material. *See* JA70, JA105–107, JA119–121. Because Micron's petition does not disclose these theories, *SAS Institute* prevents the Board from using such theories in the final decision. Accordingly, the Board's final decision should have been limited to the ground asserted in the petition, which relied solely on the etch stop structure 81 in Watatani's FIG. 5 for the

multilayer silicon nitride etch stop structure required by claims 2 and 7.

The facts here are significantly more extreme than those addressed in *Koninklijke Philips*, where the Federal Circuit found an impermissible new ground where the Board relied on Hua in combination with SMIL 1.0 rather than solely to establish the background knowledge of skilled artisans. 948 F.3d at 1334–35. Here, upon recognizing that the only combination of prior art references asserted in the petition would not have led to the combination of elements as recited in claims 2 and 7, the Board entertained a new ground that jettisoned critical aspects of the evidence and rationale of the petition in favor of a new combination based on Yota and involving different issues regarding motivations to combine.

The decision below analogizes this case to the second ground in *Koninklijke Philips*, where the skill of a skilled artisan is considered in an obviousness analysis that was found to be properly set forth. However, such an analogy does not fit this case. That ground in *Koninklijke Philips* was presented in the original petition. Here, the PTAB had to go outside of the original ground in attempting to establish that a portion of the claimed invention was in the prior art. The Federal Circuit itself recognizes this exact kind of theory shift as a new ground. *See Magnum Oil*, 829 F.3d at 1372-73, 1377; *SAS Institute, Inc. v. ComplementSoft, LLC*, 825 F.3d 1341, 1351 (Fed. Cir. 2016), *rev'd on other grounds sub nom.*, *SAS Inst., Inc. v. Iancu*, 138 S.Ct. 1348 (2018). Indeed, such changes in theory are exactly the kind that lead to inefficiencies and unfairness in a streamlined procedure like an inter partes review.

The Federal Circuit ignored the fundamental manner in which the ground changed during the trial proceeding, which is not permitted by the controlling statutory scheme, and which therefore respectfully requires review by this Court.

CONCLUSION

For the foregoing reasons, the Court should grant the petition.

Respectfully submitted.

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November 9, 2020

APPENDIX A

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

LONE STAR SILICON INNOVATIONS LLC,
Appellant

v.

ANDREI IANCU, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1669

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017- 01566.

ON PETITION FOR REHEARING EN BANC

Before PROST, *Chief Judge*, NEWMAN, LOURIE, SCHALL*, DYK, MOORE, O'MALLEY, REYNA, WALLACH, TARANTO, CHEN, HUGHES, and STOLL, *Circuit Judges*.

PER CURIAM.

O R D E R

Appellant Lone Star Silicon Innovations LLC filed a petition for rehearing en banc. The petition was first referred as a petition for rehearing to the panel that heard the appeal, and thereafter the petition for rehearing en banc was referred to the circuit judges who are in regular active service.

Upon consideration thereof, IT IS ORDERED THAT:

The petition for panel rehearing is denied. The petition for rehearing en banc is denied.

The mandate of the court will issue on June 19, 2020.

FOR THE COURT

June 12, 2020	/s/ Peter R. Marksteiner
Date	Peter R. Marksteiner
	Clerk of Court

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* Circuit Judge Schall participated only in the decision on the petition for panel rehearing.

APPENDIX B

NOTE: This disposition is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

LONE STAR SILICON INNOVATIONS LLC,
Appellant

v.

ANDREI IANCU, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1669

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01566.

Decided: March 25, 2020

TIMOTHY P. MALONEY, Fitch, Even, Tabin & Flannery, Chicago, IL, argued for appellant. Also represented by NICHOLAS T. PETERS, DAVID ALLEN GOSSE.

DANIEL KAZHDAN, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, argued for intervenor. Also

represented by MAI-TRANG DUC DANG, THOMAS W. KRAUSE, BRIAN RACILLA, FARHEENA YASMEEN RASHEED, MEREDITH HOPE SCHOENFELD.

Before LOURIE, SCHALL, and CHEN, *Circuit Judges*.

LOURIE, *Circuit Judge*

Lone Star Silicon Innovations LLC ("Lone Star") appeals from the final written decision of the Patent Trial and Appeal Board ("Board") holding claims 2 and 7 of U.S. Patent 6,388,330 (the "'330 patent") unpatentable as obvious. For the reasons described below, we *affirm*.

BACKGROUND

Lone Star is the owner of the '330 patent, which is directed to semiconductor etch stop layers with low dielectric constants. An etch stop layer is made of material that is resistant to the process used to etch other layers of a semiconductor device and is deposited between two other layers to allow those layers to be etched separately. The invention of the '330 patent reduces capacitive coupling between layers of metal interconnects by reducing the dielectric constant of the etch stop layers to below 5.5, in contrast to the prior art dielectric constants of 7.5 or higher.

Independent claims 1 and 6, which are not at issue in this appeal, are directed to integrated circuits comprising an "etch stop layer of silicon nitride . . . having a dielectric constant below 5.5." '330 patent col. 6 ll. 62–64, col. 7 ll. 22–24, col. 8 ll. 4–6. Dependent claims 2 and 7, which are at issue in this appeal, are directed to the integrated circuits of claims 1 and 6

respectively, wherein the silicon nitride etch stop layer is a "multilayer structure." *Id.* col. 7 ll. 3–4, col. 8 ll. 12–13.

Micron Technology, Inc. ("Micron") petitioned for *inter partes* review of claims 1, 2, 5, 6, 7, and 10. Micron asserted a single ground in its petition, namely, that the challenged claims were obvious over Watatani[1] in view of Tanaka.[2] The petition stated: "The Ground is explained below andis supported by the Declaration of Dr. Richard B. Fair." J.A. 70.

Within that single ground, Micron asserted two separate theories regarding the prior art's teaching of the "multilayer structure" limitation in claims 2 and 7. In its first theory, Micron contended that "Watatani expressly describes an etch stop layer that includes 'three or more layers' of silicon nitride." J.A. 105 (citing Watatani col. 7 ll. 54–55). In its second theory, Micron contended that "[s]uch multilayer silicon nitride layers were well known in the prior art," and Micron supported this second theory with declaration testimony from its expert as well as prior art references Watatani, SST 1987,[3] and Wang.[4] *See* J.A. 105–07; *see also* J.A. 81–82 ("It Was Well Known In The Prior Art To Form Multilayer Silicon Nitride Etch Stop Films").

The Board instituted review of the challenged

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[1] U.S. Patent 6,153,511.

[2] Masayuki Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, *in* 1999 SYMPOSIUM ON VLSI TECHNOLOGY, DIGEST OF TECHNICAL PAPERS, 47–48 (Bus. Center for Acad. Societies Japan, 1999).

[3] Novellus Sys., *Continuous Process CVD System*, 30 SOLID STATE TECH., no. 10, Oct. 1987, at 49–50.

[4] U.S. Patent 6,017,791.

claims. J.A. 209. For the "multilayer structure" of claims 2 and 7, the Board rejected Micron's first theory, *i.e.*, the theory based on the description in Watatani. J.A. 224 ("On this record, we agree with Patent Owner that Watatani does not describe an etch stop layer that includes three or more layers of silicon nitride."). But the Board expressly acknowledged that Micron had asserted a second independent theory for the "multilayer structure" limitation:

> Petitioner's contentions regarding claims 2 and 7 are not, however, based solely on Watatani's disclosure of multilayer etch stops. Petitioner also contends that "multilayer silicon nitride layers were well known in the prior art."

J.A. 225. The Board found that Micron's evidence—including the teachings of SST 1987 and Wang—was "sufficient to support its contention that multilayer silicon nitride layers were known in the art." J.A. 226.

Lone Star filed a request for rehearing, arguing that the Board exceeded its authority by instituting review of claims 2 and 7 "based on a new ground not asserted in the Petition." J.A. 241. The Board denied Lone Star's request, finding that the institution decision relied on additional prior art references "in the same way" that Micron's petition did, namely, "as evidence of the knowledge of a person of ordinary skill in the art." J.A. 258. The Board noted that Lone Star "cites no authority for the proposition that a reference relied upon to show that a claim limitation is within the knowledge of a [person of ordinary skill in the art] must be expressly included in the list of references that denominate the ground." J.A. 259; *see* J.A. 258 ("Our reliance on SST 1987, however, does not transform the instituted ground into a 'new ground,' as argued by Patent Owner.").

In its patent owner response, Lone Star again raised its contention that the Board had exceeded its authority and also addressed the merits of the obviousness challenge. Micron argued in reply that the instituted ground based on Watatani, Tanaka, and the knowledge of a person of ordinary skill had been asserted in the petition. J.A. 378–80. Micron also submitted a second declaration from its expert declarant, Dr. Fair, who cited yet another reference, Yota,[5] to support his opinion that that multilayer silicon nitride films were well-known in the art. *See* J.A. 890–94.

Lone Star believed that portions of Micron's reply improperly relied on new evidence, particularly those por- tions that relied on Dr. Fair's citations to additional exhibits, such as Yota, that were not previously submitted with Micron's petition. *See* J.A. 1483–85. The parties jointly requested permission from the Board to submit additional briefing, which the Board allowed. *Id.* Lone Star thus had the opportunity to submit a sur-reply in which it addressed Dr. Fair's second declaration, including his reliance on Yota. *See* J.A. 397–99.

In its final written decision, the Board held all of the challenged claims, including claims 2 and 7, obvious over Watatani in view of Tanaka. J.A. 2. The Board again rejected Lone Star's argument that the Board had exceeded its authority and again emphasized that its institution decision and final written decision properly relied on additional references like SST 1987 "in the *same way* as it was

[5] Jiro Yota et al., *Comparison between HDP CVD and PECVD Silicon Nitride for Advanced Interconnect Applications*, *in* PROC. OF THE IEEE 2000 INT'L INTERCONNECT TECH. CONFERENCE, 76–78 (IEEE Electron Devices Soc'y, 2000).

relied upon in the Petition: as evidence that multilayer silicon nitride layers were known in the prior art." J.A. 42. On the merits, the Board held that Micron proved by a preponderance of the evidence that a person of ordinary skill in the art would have been motivated to use a multilayer silicon nitride structure when forming an etch stop layer and would have had a reasonable expectation of success in achieving the subject matter of claims 2 and 7. J.A. 38–39.

Lone Star appealed the Board's final written decision only with respect to claims 2 and 7. Micron declined to participate in the appeal because it had already reached a settlement with Lone Star. The Director of the United States Patent and Trademark Office ("Director") intervened pursuant to 35 U.S.C. § 143. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

Our review of a Board decision is limited. *In re Baxter Int'l, Inc.*, 678 F.3d 1357, 1361 (Fed. Cir. 2012). We review the Board's legal determinations *de novo*, *In re Elsner*, 381 F.3d 1125, 1127 (Fed. Cir. 2004), but we review the Board's factual findings underlying those determinations for substantial evidence, *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). A finding is supported by substantial evidence if a reasonable mind might accept the evidence as adequate to support the finding. *Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229 (1938). "Where there is adequate and substantial evidence to support either of two contrary findings of fact, the one chosen by the board is binding on the court regardless of how we might have decided the issue if it had been raised *de novo*." *Mishara Constr. Co. v. United States*, 230 Ct.

Cl. 1008, 1009 (1982) (citing *Koppers Co. v. United States*, 186 Ct. Cl. 142, 151 (1968), *and Nat'l Concrete & Found. Co. v. United States*, 170 Ct. Cl. 470, 478 (1965)).

Lone Star raises two challenges on appeal. First, Lone Star contends that the Board exceeded its authority when it reviewed claims 2 and 7 and held them unpatentable based on a ground of obviousness that was not asserted in Micron's petition for inter partes review. Second, Lone Star contends that the Board's obviousness conclusion for claims 2 and 7 is not supported by substantial evidence. We address Lone Star's challenges in turn.

I

Lone Star argues that the petition set forth a single ground of obviousness based solely on the combination of Watatani and Tanaka, but the Board held the claims unpatentable based on an unasserted ground that included a combination of those two references with at least three additional references—SST 1987, Wang, and Yota. According to Lone Star, the Board exceeded its authority, as set forth in 37 C.F.R. § 42.108(a), to authorize review to proceed on "all or some of the *grounds* of unpatentability asserted for each claim." Appellant Br. 37 (quoting and adding emphasis to the regulation).

The Director responds that Lone Star is attempting to challenge the Board's institution decision, which is a nonappealable issue pursuant to 35 U.S.C. § 314(d). The Director further argues that, even to the extent that Lone Star's challenge is appealable, the Board did not abuse its discretion or exceed its authority in this case.

We agree with the Director that Lone Star's challenge is directed to the Board's institution

decision, which is not appealable. The relevant statutory language is the "No Appeal" clause in Section 314(d):

> **(d) No Appeal.**—The determination by the Director whether to institute an inter partes review under this section shall be final and nonappealable.

In *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2141 (2016) ("*Cuozzo III*"), the Supreme Court held that "[t]he text of the 'No Appeal' provision, along with its place in the overall statutory scheme, its role alongside the Administrative Procedure Act, the prior interpretation of similar patent statutes, and Congress' purpose in crafting inter partes review, all point in favor of precluding review of the Patent Office's institution decisions."

We recently addressed a challenge similar to the one presented here. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330 (Fed. Cir. 2020). In that case, the petition presented a single obviousness ground based on the SMIL reference but also relied on the Hua reference as evidence of what was known in the art. *Id.* at 1333–34. Although the petition asserted only one obviousness ground, the Board instituted review on two obviousness grounds—(1) SMIL in view of Hua and (2) SMIL "in light of the *general* knowledge of the skilled artisan." *Id.* at 1334. Regarding the first instituted ground, we concluded that it was error for the Board to institute review based on a ground of obviousness over SMIL and Hua because that ground was not presented in the petition. *Id.* at 1337. But regarding the second instituted ground, we found no error in the Board's decision to institute review based on obviousness over SMIL in view of the knowledge of a person of ordinary skill. *Id.* at 1338. Notably, the evidence presented to support the knowledge of a

person of skill relied in part on other references, including Hua.

Here, like the second instituted ground in *Koninklijke Philips*, the Board instituted inter partes review based on the ground of obviousness that was presented in Micron's petition—Watatani in view of Tanaka. The petition undisputedly asserted only one obviousness ground. The Board was not, however, obligated to "ignore the skilled artisan's knowledge when determining whether it would have been obvious to modify the prior art." *Id.* at 1337. Indeed, the statutory definition of obviousness expressly depends on what would have been known to a person having ordinary skill in the art. 35 U.S.C. § 103.

Lone Star focuses entirely on the listed references. Lone Star insists that the instituted ground was not actually presented in the petition because it relies on additional references beyond Watatani and Tanaka that were not presented in the petition and the Board lacked authority to *sua sponte* add its own ground of unpatentability. Lone Star argues that the mere fact that the Board failed to explicitly acknowledge this as a "new ground" is insufficient to distinguish this case from the first instituted ground in *Koninklijke Philips*, which we found to be instituted in error. 948 F.3d at 1337. But here, the Board repeatedly made clear that the instituted ground was based on Watatani and Tanaka, and that the additional references were being relied on exclusively for their teachings about what was well-known in the art. J.A. 225; *see also* J.A. 42, 258. And the Board only did so after it expressly interpreted the petition to have presented that argument. *E.g.* J.A. 225 (quoting "*[p]etitioner's* contention[] that 'multilayer silicon nitride layers were well known in the prior art.'" (emphasis added)); J.A. 226 ("*Petitioner's* evidence is sufficient to support

its contention . . . ."). Under Section 314(d), the Board's decision to institute review based on its interpretation of the petition is not appealable. *See Cuozzo III*, 136 S. Ct. at 2139 (holding that the Board's interpretation of the petition to have implicitly presented a challenge was unreviewable).

Lone Star attempts to avoid the "No Appeal" clause by arguing that its challenge in this case is not to the Board's institution decision, but rather to the scope of the Board's statutory and regulatory authority throughout the proceeding, which is reviewable. Lone Star relies heavily on the Supreme Court's acknowledgment that the petition is "the centerpiece of the proceeding both before and after institution." *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1358 (2018). Lone Star argues that the "No Appeal" clause in Section 314(d) pertains only to the "preliminary patentability [decision]" based on the "patentability merits of particular claims," and is thus inapplicable in this case. *See* Reply Br. 6 (quoting *Wi-Fi One, LLC v. Broadcom Corp.*, 878 F.3d 1364, 1372 (Fed. Cir. 2018) (en banc)). According to Lone Star, the controlling authority in this case is 37 C.F.R. § 42.108, which allows the Board to institute review "on all or some of the grounds of unpatentability asserted." Lone Star also argues that 35 U.S.C. § 311(b) limits the scope of the Board's authority to a ground on which a petitioner asks for review.

We disagree with Lone Star's characterization of both its challenge and the Board's institution decision. In *Cuozzo III*, the Supreme Court held that the "No Appeal" clause applies to attacks that are "closely tied" to the Board's "decision to initiate inter partes review." 136 S. Ct. at 2141. We find that this is such a case. In order to grant the relief that Lone Star requests, we would have to unwind the Board's

institution decision and compare it to the particular language used in Micron's petition regarding the "multilayer structure" limitation, which is precisely the kind of analysis the Supreme Court cautioned against. *Id.* at 2139. In essence, Lone Star's argument that a specific theory was not within "the grounds of unpatentability asserted" under 37 C.F.R. § 42.108 "is little more than a challenge to the Patent Office's conclusion, under § 314(a), that the 'information presented in the petition' warranted review." *Id.* at 2142.

In an attempt to distinguish *Cuozzo III*, Lone Star points to a number of cases in which this court has reviewed institution-stage issues. But in each such case the reviewable issue was not closely tied to substantive patentability requirements. *See Arista Networks, Inc. v. Cisco Sys., Inc.*, 908 F.3d 792, 799 (Fed. Cir. 2018) (reviewing assignor estoppel); *Wi-Fi One*, 878 F.3d 1364, 1374 (reviewing time bar); *see generally Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336 (Fed. Cir. 2018) (reviewing the real party in interest requirement). And while the Supreme Court itself acknowledged that the "No Appeal" clause does not extend to appealable constitutional or statutory violations, *Cuozzo III*, 136 S. Ct. at 2141–42, that acknowledgement is not applicable here, where Lone Star's challenge is to the evidentiary basis underpinning the Board's interpretation of the petition in its institution decision.

We also note that that this court has entertained challenges to the Board for exceeding its authority in violation of the Administrative Procedure Act ("APA") by, for example, failing to give "notice of and a fair opportunity to meet the grounds of rejection." *In re NuVasive, Inc.*, 841 F.3d 966, 971 (Fed. Cir. 2016)

(quoting *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1080 (Fed. Cir. 2015)). But, importantly, Lone Star has not raised such a challenge under the APA in this case. Indeed, the crux of Lone Star's argument is that the Board exceeded its authority notwithstanding the undisputed fact that Lone Star *did* have notice of the full scope of the inter partes review and an adequate opportunity to respond in its patent owner response and its sur-reply. In the context of challenges under the APA, we have found that the Board is within its authority to institute review and consider even arguments that were *not* asserted in the petition "after giving [the patent owner] a full opportunity to submit additional evidence and arguments on that point." *NuVasive*, 841 F.3d at 975 (citing *In re Kumar*, 418 F.3d 1361, 1367–69 (Fed. Cir. 2005)). All the more so here, where the Board put Lone Star on notice of its finding that the "multilayer structure" theory *was* presented in the petition, there is nothing in the patent statute or the regulations that limits the Board's authority to include that theory within the scope of its re- view. [6]

At bottom, the Board interpreted the petition to have presented a specific theory for the "multilayer structure" limitation. The Board instituted an inter partes review that includes that theory. Lone Star asks us to review that institution decision. Under the "No Appeal" clause, as interpreted by the Supreme Court in *Cuozzo III*, that decision is not reviewable.

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[6] Although not cited in the petition, Yota was not needed for the petition to establish, on the basis of SST 1987 and Wang, that multilayer silicon nitride structures were well known. To the extent that the Board relied on Yota to rebut specific arguments made by Lone Star against reasonable expectation of success, the Board was within its authority to do so where Lone Star was given ample opportunity to respond.

II

We turn now to Lone Star's challenge on the merits of the Board's obviousness conclusion for claims 2 and 7. Obviousness is a question of law based on underlying facts, including the scope and content of the prior art, differences between the prior art and the claims at issue, the level of ordinary skill, and relevant evidence of secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Whether a skilled artisan would have been motivated to combine prior art references is also a question of fact. *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1238–39 (Fed. Cir. 2010).

Lone Star challenges a number of the facts underlying the Board's obviousness conclusion. Lone Star contends that, even accepting that a multilayer structure of silicon nitride was well-known in the art, the record is devoid of evidence that such a multilayer structure was known tobe used *as an etch stop layer*, which is what claims 2 and 7 actually require. Lone Star also challenges the Board's conclusions regarding motivation to combine and reasonable expectation of success. Lone Star argues that the two alleged motivations to use a multilayer structure—layer uniformity and avoiding pinholes—are divorced from the overall context of the claims, which require that the etch stop layer have a dielectric constant below 5.5. And Lone Star argues that the evidence in the record demonstrates that a person of skill would have expected a multilayer structure to increase the dielectric constant of the etch stop layer, which is the opposite of the claimed invention directed to lower dielectric constants.

The Director responds that the multilayer structure limitation of claims 2 and 7 adds no patentable significance to the obvious integrated

circuit of claims 1 and 6. Said differently, the Director argues that claims 2 and 7 are directed to nothing more than starting with an obvious integrated circuit and adding a well-known multilayer structure that has well-established benefits for integrated circuits. The Director further argues that Lone Star's motivation to combine argument is contrary to law, and that substantial evidence from both parties' experts and multiple prior art references supports the Board's findings regarding reasonable expectation of success.

We agree with the Director. The Supreme Court has made clear that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). For purposes of this appeal, it is not disputed that multilayer structures were known to improve integrated circuits by improving layer uniformity and decreasing pinholes. And the record contains substantial evidence that using the multilayer structure of silicon nitride recited in claims 2 and 7 would improve the etch stop layers in the integrated circuits of claims 1 and 6 in the same way. Thus, the multilayer structure does not ren- der nonobvious the otherwise obvious integrated circuits of claims 1 and 6.

Furthermore, regarding a motivation to combine, we reject Lone Star's contention that the known advantages that would have motivated a person of skill to use multilayer structures must be shown to directly impact the claimed lower dielectric constant. On the contrary, the law is clear that "the motivation to modify a prior art reference to arrive at the claimed

invention *need not* be the same motivation that the patentee had." *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1347 (Fed. Cir. 2018) (citation omitted, emphasis added). Here, there is substantial evidence that a person of skill would have been motivated to use a multilayer structure of silicon nitride as an etch stop layer to improve layer uniformity and avoid pinholes. And, having been motivated to use a multilayer structure, the person of skill would have thus arrived at the claimed invention of claims 2 and 7.

Finally, regarding the reasonable expectation of successfully achieving a low dielectric constant with a multilayer structure, the Board relied on the testimony of both parties' expert witnesses regarding the relationship between density and dielectric constants when stacking multiple thin layers to achieve thickness. J.A. 41–42 (citing both Dr. Fair and Dr. Bottoms). And simply put, the Tanaka prior art reference teaches a silicon nitride layer with a dielectric constant that is below 5.5 as required by the claims, *see* J.A. 41, and Micron's expert, Dr. Fair, pointed to multiple references to support his opinion that the low dielectric constant could be maintained using a multilayer structure. J.A. 893–94. Lone Star challenged Dr. Fair's opinions below with the same factual arguments it now raises on appeal, but the Board rejected Lone Star's challenges based on the teachings of the prior art references, the background of the '330 patent itself, and inconsistencies within Lone Star's positions. J.A. 47–48. We are not in a position to second-guess the Board's evaluation of expert witnesses' credibility or its reconciliation of perceived inconsistencies in their testimony. *Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) ("We defer to the Board's findings concerning the credibility of

expert witnesses." (citing *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003))). On this record, the Board's finding that a person of skill would have had a reasonable expectation of successfully achieving the invention of claims 2 and 7 is supported by substantial evidence.

CONCLUSION

We have considered Lone Star's remaining arguments, but we find them to be unpersuasive. Accordingly, the decision of the Board holding unpatentable claims 2 and 7 of the '330 patent is affirmed.

AFFIRMED

APPENDIX C

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,
v.
LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01566
Patent 6,388,330 B1

Before JON B. TORNQUIST, JOHN F. HORVATH, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

Micron Technology, Inc. ("Petitioner") challenges the patentability of claims 1, 2, 5–7, and 10 ("the challenged claims") of U.S. Patent No. 6,388,330 B1 (Ex. 1001, "the '330 patent"), assigned to Lone Star Silicon Innovations, LLC ("Patent Owner").[1]

We have jurisdiction under 35 U.S.C. § 6. This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that the challenged claims of the '330 patent are unpatentable.

I. BACKGROUND

A. Procedural History

Petitioner filed a Petition seeking *inter partes* review. Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp."). We instituted *inter partes* review of all challenged claims of the '330 patent. Paper 8 ("Institution Decision" or "Dec."). Patent Owner's Request for Rehearing (Paper 10) was denied. Paper 11 ("Rehearing Decision" or "Reh'g Dec.")

Patent Owner filed a Response. Paper 14 ("PO Resp."). Petitioner filed a Reply. Paper 16 ("Pet. Reply"). With the Board's prior authorization (Ex. 2014), Patent Owner filed a Sur-Reply addressing limited issues. Paper 17 ("PO Sur-Reply"). Pursuant to the same authorization, Petitioner filed a Sur-Sur-Reply. Paper 21 ("Pet. Sur-Sur-Reply").

With the Petition, Petitioner filed a declaration of Richard Fair, Ph.D. Ex. 1003. Patent Owner cross-

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[1] Patent Owner identifies Longhorn IP LLC as an additional real party-in- interest. Paper 18, 1.

examined Dr. Fair and filed a transcript of his deposition testimony as Exhibit 2009 with the Patent Owner Response.

With the Reply, Petitioner filed a second declaration of Dr. Fair. Ex. 1017. With the Preliminary Response, Patent Owner filed a declaration of Wilmer R. Bottoms, Ph.D. Ex. 2001. With the Patent Owner Response, Patent Owner filed a second declaration of Dr. Bottoms. Ex. 2008. Petitioner cross-examined Dr. Bottoms and filed a transcript of his deposition testimony as Exhibit 1018 with Petitioner's Reply. With its Sur- Reply, Patent Owner filed a third declaration of Dr. Bottoms. Ex. 2015.

Oral argument was held October 11, 2018. A transcript of the oral argument was entered in the record. Paper 23 ("Tr.").

B. Related Matters

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following pending federal court proceedings involving the '330 patent: *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, Appeal No. 2018-1578 (Fed. Cir., filed Feb. 15, 2018) and *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (N.D. Cal., filed Mar. 16, 2018). Paper 18, 2–3. In addition, Patent Owner identifies Federal Circuit Appeal Nos. 2018-1580, 2018-1581, and 2018-1582, in which the defendant-appellees are Renesas Electronics Corp., Nanya Technology Corp., and United Microelectronics Corp., respectively. *Id.*

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following *inter partes* review proceedings involving the '330 patent: *Renesas*

Electronics Corp. v. Lone Star Silicon Innovations, LLC, Case IPR2017-01869 and *Nanya Technology Corp. v. Lone Star Silicon Innovations, LLC*, Case IPR2018-00062. Paper 18, 2.

C. The '330 Patent (Ex. 1001)

The '330 patent is titled "Low Dielectric Constant Etch Stop Layers in Integrated Circuit Interconnects" and was issued May 14, 2002, from Application No. 09/776,012, filed February 1, 2001. Ex. 1001 at (21), (22), (45), (54).

The '330 patent relates to semiconductor technology and, more specifically, to etch stop layers in integrated circuits. *Id.* at 1:6–8. According to the '330 patent, semiconductor devices fabricated in and on a semiconductor substrate may be interconnected using a "damascene" technique of metallization. *Id.* at 1:11–29. A "single damascene" technique forms a single layer of conductive interconnects, and a "dual damascene" technique forms multiple layers of conductive interconnects that are separated by interlayer dielectric layers, including etch stop layers, in vertically separated planes and interconnected by vertical connections or "vias." *Id.* at 1:30–34, 2:30–51. The '330 patent discloses that closely positioned, parallel conductive channels suffer from capacitive coupling effects, which can be reduced by reducing the dielectric constant of the silicon nitride etch stop layers between the channels. *Id.* at 3:32–42, 3:49–60. More specifically, the '330 patent represents that "currently used silicon nitride . . . has a dielectric constant in excess of 7.5" (*id.* at 3:39–41) and discloses that capacitive coupling effects are reduced by using an etch stop layer having a dielectric constant below 5.5 (*id.* at 3:53–54, 3:58–59).

Figure 2 of the ’330 patent shows a “prior art” structure, and Figure 3 shows the invention. Ex. 1001, 4:14–20. Figures 2 and 3 of the ’330 patent are reproduced below:

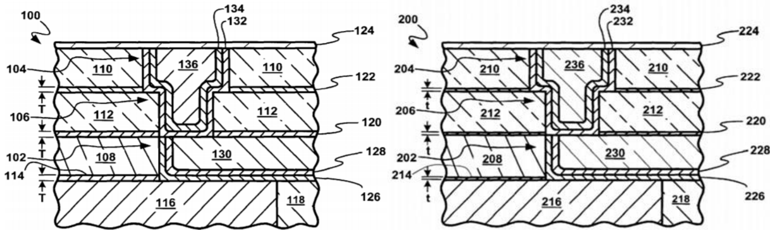

FIG. 2 (PRIOR ART)

FIG. 3

Figures 2 and 3, above, show semiconductor wafers 100, 200, including dielectric layers 108, 110, 112, 208, 210, and 212; conductor cores 130, 136, 230, 236; and etch stop layers 114, 120, 122, 124, 214, 220, 222, and 224.[2] *Id.* at 4:24–32, 4:42–5:4, 5:21–53. According to the ’330 patent, Figure 3 is “similar” to Figure 2, except for the thickness of the etch stop layers, which is shown as “T” in Figure 2 and “t” in Figure 3. *Id.* at 4:18, 5:17–23, 5:66–6:2.

Regarding the etch stop layers, the ’330 patent discloses:

> In the present invention, a half thickness, high quality, etch stop layer (compared to the prior art etch stop layer) is deposited.
>
> For example, for silicon nitride, the dielectric constant of an etch stop layer in accordance with the present invention is about 5.5 contrasted to an excess of 7.5 in the prior art.

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[2] Structures with 100-series reference numerals are shown in Figure 2, and structures with 200-series reference numerals are shown in Figure 3.

Id. at 5:60–65. The ’330 patent discloses processes that can be used to produce etch stop layers with a dielectric constant under 5.5, including successive deposition of multiple layers of silicon nitride, which “eliminates pinholes and produces a denser film.” *Id.* at 5:66–6:7.

D. Illustrative Claim

The Petition challenges claims 1, 2, 5–7, and 10, of which claims 1 and 6 are independent. Ex. 1001, 8:57–12:35. Claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. An integrated circuit comprising:
>
> a semiconductor substrate having a semiconductor device provided thereon;
>
> a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;
>
> a first conductor core filling the first opening and connected to the semiconductor device;
>
> an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5;
>
> a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core;
>
> a second conductor core filling the second opening and connected to the first conductor core.

Ex. 1001, 6:54–7:2.

Claim 6 is similar to claim 1, except that it recites

an additional dielectric layer (called a via dielectric layer) and an additional etch stop layer (called a channel etch stop layer), and the second conductor core fills openings in both the via and second dielectric layers. *Id.* at 7:15–8:11.

E. Instituted Ground of Unpatentability

We instituted *inter partes* review based on the sole ground of unpatentability asserted in the Petition: whether claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Watatani[3] and Tanaka I.[4] Dec. 20.

II. ANALYSIS

A. Claim Construction

In this *inter partes* review, the '330 patent has not yet expired, and claim terms are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2016).[5] Under that standard, we generally

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[3] Watatani, US 6,153,511, filed June 25, 1999, and issued November 28, 2000, Ex. 1005 ("Watatani"). Watatani is asserted as prior art under 35 U.S.C. § 102(e). Pet. 25 n.7.

[4] Masayuki Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47–48, Ex. 1006 ("Tanaka I"). Tanaka I is asserted as prior art under 35 U.S.C. § 102(b). Pet. 27 n.8. Petitioner relies on the Declaration of Peter J. Rolla, an employee of the University of California San Diego Library in La Jolla, California, to establish public accessibility of Tanaka I. Ex. 1009.

[5] A recent amendment to this rule does not apply here, because the Petition was filed before November 13, 2018. *See* "Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board," 83 Fed. Reg. 51,340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42).

give claim terms their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In the Institution Decision, we determined it was not necessary to resolve any claim construction disputes for purposes of that decision. Dec. 7–8. Neither party challenges that determination. Patent Owner continues to argue that the phrase "etch stop layer of silicon nitride" is not limited to a layer of pure silicon nitride and allows for the presence of dopants and/or impurities. *Compare* PO Resp. 12–15, *with* Prelim. Resp. 15–20. Petitioner argues there is no controversy in this proceeding to which Patent Owner's proposed construction is relevant. Pet Reply 1. We agree, as Patent Owner does not rely on its proposed claim construction for any patentability argument. In fact, Patent Owner relies on the assertions of Petitioner and Dr. Fair regarding one of the asserted prior art references—Tanaka I (Ex. 1006)—as support for Patent Owner's claim construction. PO Resp. 15. More particularly, Patent Owner concedes that the silicon nitride etch stop layer disclosed in Tanaka I, which contains hydrogen and chlorine impurities, is an "etch stop layer of silicon nitride" within the meaning of claims 1 and 6. *Id.* Under these circumstances, we do not need to provide an express construction for the phrase "etch stop layer of silicon nitride" for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc.*

v. Am. Sci. & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Principles of Law

Petitioner bears the burden of proving unpatentability, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish the facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In this case, neither party relies on objective evidence of nonobviousness, i.e., secondary considerations.

C. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Fair, testifies that a person of ordinary skill in the art ("POSA") would have had at least a Bachelor of Science degree in electrical engineering, material science, physics, chemistry, or a closely related field, and at least five years of industry experience in the development of

semiconductor process technologies and the fabrication of semiconductor devices. Ex. 1003 ¶ 18. Dr. Fair further testifies that an individual with an advanced degree in a relevant field would require less experience in developing process technologies and in fabricating semiconductor devices. *Id.* Patent Owner's declarant, Dr. Bottoms, testifies that a POSA would have held a master's degree in physics, electrical engineering, or a related field, and would have had three years or more experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. Ex. 2008 ¶ 29.

For purposes of our Institution Decision, we accepted the description of a POSA provided by Dr. Bottoms. Dec. 8 (citing Ex. 2001 ¶ 33). Dr. Bottoms testifies that his description does not differ significantly from Dr. Fair's. Ex. 2008 ¶ 29. Dr. Fair testifies that Dr. Bottoms' description of the level of ordinary skill in the art is consistent with the level proposed in his original declaration, and the Board's adoption of that description does not change his opinions. Ex. 1017 ¶ 5.

Consistent with the testimony of Dr. Fair and Dr. Bottoms, we find there is little difference between the descriptions of a POSA, and the outcome of our patentability determinations would be the same, regardless of which description we accept. Therefore, consistent with the Institution Decision, we adopt Dr. Bottoms' description of a POSA. Ex. 2008 ¶ 29. We also rely on the cited prior art references as reflecting the level of ordinary skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

After reviewing the qualifications of Dr. Fair and

Dr. Bottoms, as set forth in each witness's declaration and curriculum vitae ("CV"), we find that each of these declarants has sufficient education and experience related to the subject matter of the '330 patent to testify from the perspective of a POSA at the time of the invention. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2008 ¶¶ 6–17. *See* Trial Practice Guide Update," 83 Fed. Reg. 38,989 (Aug. 13, 2018), *available at* https://go.usa.gov/xU7GP ("TPG Update"), 3 ("A person may not need to be a person of ordinary skill in the art in order to testify as an expert under Rule 702, but rather must be "qualified in the pertinent art."" (quoting *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008))). Regarding the qualifications of Dr. Fair, we find particularly relevant his experience as an acting president, vice president, and director at the Microelectronics Center of North Carolina ("MCNC") from 1981 to 1994, where he directed research on semiconductor processing, including photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD (chemical vapor deposition) of thin films, metallization, and anisotropic etching processes, and conducted research on multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, and selective tungsten deposition for via filling. Ex. 1003 ¶ 9, Ex. 1004, 3. Regarding the qualifications of Dr. Bottoms, we find particularly relevant his experience at Varian Associates from 1976 to 1985, including his experience as Manager of Research and Development, where he was involved in developing tools used to fabricate semiconductor devices

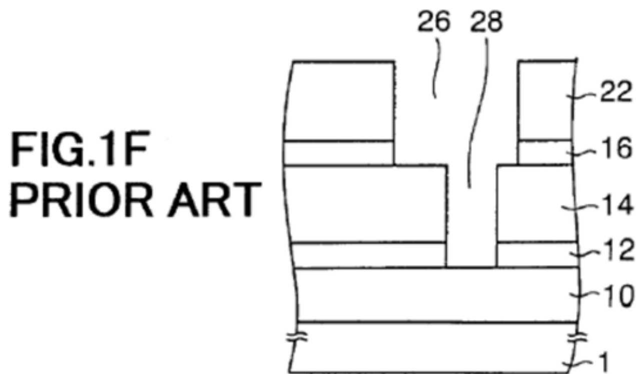
including lithography, sputtering, ion implantation, etching, and evaporation processes. Ex. 2008 ¶¶ 9–11; Ex. 2002, 1.

Petitioner argues that we should credit Dr. Fair's testimony and reject Dr. Bottoms' testimony because "Dr. Bottoms' expertise in the field pales in comparison to Dr. Fair's." Pet. Reply 18. Petitioner bases its argument on Dr. Bottoms' response to a deposition question regarding "Fick's laws of diffusion" and a comparison of the number of papers and conference presentations for the period 1984 to 2004 listed on each declarant's CV. *Id.* (citing Ex. 1004, 3–16; Ex. 1018, 9:20–24; Ex. 2002, 6–7). Petitioner's argument does not persuade us to reject Dr. Bottoms' testimony. In our view, Dr. Bottoms' inability to recall a name (Fick) associated with a particular scientific principle does not prove a lack of expertise in the technologies relevant to this proceeding. Furthermore, the number of papers and conference presentations listed on Dr. Bottoms' CV is not the sole, or necessarily the best, measure of his level of expertise. The number of such items may depend on the institutional setting in which he worked, e.g., in industry rather than academia. Dr. Bottoms explains that his CV lists selected presentations and publications and omits some data for the relevant time period. Ex. 2015 ¶¶ 2–4. On this record, we find that Dr. Fair and Dr. Bottoms both have sufficient education and experience related to the subject matter of the '330 patent to testify regarding the knowledge and understanding of a POSA at the time of the invention and that, even if he is not a POSA, Dr. Bottoms' testimony is helpful to the Board. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2008 ¶¶ 6–17. *See* TPG Update, 3.

D. Prior Art References

1. Watatani (Ex. 1005)

Watatani discloses a semiconductor device having a multilayer interconnection structure. Ex. 1005 at (54). According to Watatani, Figures 1A–F "show a typical example of the conventional dual damascene process of forming a multilayer interconnection structure . . . ." *Id.* at 1:65–67. Petitioner relies on Watatani Figure 1F, which is reproduced below:



Watatani Figure 1F illustrates a structure resulting from a processing step in a conventional dual damascene process. Ex. 1005, 1:65–67, 2:43–48, 5:32–33. The structures shown in Watatani Figure 1F include silicon (Si) substrate 1, lower interconnection pattern 10 of conductive material such as copper (Cu), etching stopper film 12 of silicon nitride (SiN), first interlayer insulation film 14 of silicon oxide (SiO_2), second etching stopper film 16 of SiN, second interlayer insulation film 22 of SiO_2, interconnection groove 26, and contact hole 28. *Id.* at 2:1–41. According to Watatani, "an insulation film (not illustrated) [is] interposed between the Si substrate 1 and the lower interconnection pattern 10." *Id.* at 2:3–5. Watatani discloses that

interconnection groove 26 and contact hole 28 are filled with copper (Cu). *Id.* at 2:42–47.

According to Watatani, the multilayer interconnection structure of Figure 1F "has a drawback, due to the use of SiO_2 having a large dielectric constant, for the interlayer insulation film 14 or 22, in that the interconnection patterns tend to have a large stray capacitance." Ex. 1005, 2:54–58. Watatani discloses that this problem is overcome by using "an organic interlayer insulation film having a characteristically small dielectric constant." *Id.* at 2:61–64. Watatani states, however, that conventional multilayer interconnection structures using an organic interlayer insulation film also suffer from a drawback, namely, that resist pattern misalignments are difficult to correct. Ex. 1005, 3:51–4:41. To address the resist pattern misalignment problem, Watatani discloses a semiconductor fabrication process that includes the steps of forming a first etching stopper film on an organic interlayer insulation film and forming a second, different etching stopper film on the first etching stopper film. *Id.* at 4:48–5:25; *see also id.* at 6:4–10 (disclosing "an etching stopper structure 81, formed of a stacking of two etching stopper layers, . . . a first etching stopper film 80 of SiN . . . and a second etching stopper film 82 of SiO_2"); Fig. 5A.

2. Tanaka I (Ex. 1006)

Tanaka I addresses the problem of parasitic capacitance associated with copper (Cu) interconnects formed by a conventional damascene process that uses high-k SiN film for the etch stopper layers. Ex. 1006, 1-1.[6,7] To solve this

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[6] We cite to Tanaka I and other non-patent references using the

problem, Tanaka I discloses a "[n]ew low-k SiN film with a permittivity of 5.4 and high immunity for Cu diffusion and oxidation ...." *Id.* at 1-1, 1-2. The film is formed by an ultra-low temperature thermal chemical vapor deposition ("CVD") process using HexaChloroDisilane (HCD, Si_2Cl_6) as a silicon source. *Id.* at 1-1. Tanaka I refers to the new film as "HCD-SiN" and discloses a deposition process and film properties for the new film. *Id.* at 1-1, 1-2, Figs. 2–8.

Figure 1 of Tanaka I is reproduced below:

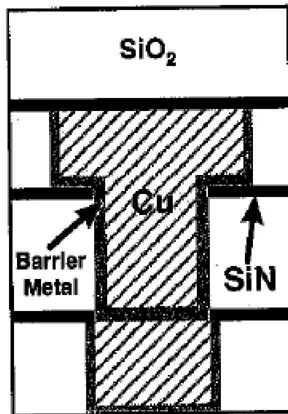

Fig.1 A schematic drawing of Cu interconnects formed by damascene process

Figure 1 of Tanaka I shows copper interconnects formed by a conventional dual damascene process, which requires "plural layers of high-k SiN film for a

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page numbers added by Petitioner or Patent Owner followed by a hyphenated suffix ("-1," "-2," or "-3") to indicate the first, second, or third column.

[7] Dr. Fair explains that "[t]he dielectric constant of a material, which is sometimes referred to as its permittivity and which is represented by the letter 'k,' is an intrinsic property of a material . . . ." Ex. 1003, 19 n.2.

groove etch stopper and a barrier of Cu diffusion and oxidation ....” Ex. 1006, 1-1. As explained above, Tanaka I proposes improving upon this conventional process by using “HCD-SiN as the etch-stop and the barrier layer ... to realize Cu damascene interconnects for high performance VLSIs.”[8] *Id.*

E. Petitioner’s Obviousness Ground

Petitioner contends that claims 1, 2, 5–7, and 10 of the ’330 patent are unpatentable as obvious in view of Watatani and Tanaka I. Pet. 29–38, 42–53. We address each of the challenged claims below.

1. Claims 1 and 6

Petitioner contends that the conventional dual damascene interconnect structure of Watatani teaches or suggests all elements of independent claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 29–38, 42–53. Petitioner acknowledges that Watatani does not disclose the dielectric constant of the silicon nitride etch stop layer and relies on Tanaka I for that feature. *Id.* at 35–36, 48, 51. Petitioner contends that a POSA would have been motivated to use Watatani’s conventional dual damascene interconnect structure, labeled as a prior art structure, but use Tanaka I’s low-k silicon nitride etch stop layers instead of conventional silicon nitride etch stop layers in order to minimize the stray capacitance issue discussed in both references. *Id.* at 29, 36. Petitioner contends that a POSA would have been motivated to combine the teachings of Watatani and Tanaka I and would have had a reasonable expectation of success in doing so. *Id.* at

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[8] The acronym VLSI refers to very large scale integrated devices. *See* Ex. 1013, 1.

13–15, 36, 48–49, 51–52, 56–60.

Patent Owner argues that Watatani does not disclose an etch stop layer formed over the first dielectric layer, as recited in the claims. PO Resp. 35. In addition, Patent Owner challenges the sufficiency of the evidence to establish motivation and a reasonable expectation of success for the combination of Watatani's damascene structure with Tanaka I's low dielectric constant silicon nitride. *Id.* at 35–53.

Petitioner directs us to substantial evidence that Watatani's conventional dual damascene structure (Ex. 1005, 1:65–2:47, Figs. 1A–F) discloses all limitations of claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 29–34, 37–38, 42–47, 49–50, 52–53. Patent Owner does not contest that evidence, except to argue that Watatani does not disclose an etch stop layer formed over the first dielectric layer, an argument we address in section II.E.1.a below. *See* PO Resp. 35. We determine Petitioner has shown by a preponderance of the evidence that all of the uncontested limitations of claims 1 and 6 are disclosed by Watatani and, in some cases, also by Tanaka I. Pet. 29–34, 37–38, 42–47, 49–50, 52–53. The remainder of our analysis focuses on the contested limitations of claims 1 and 6, i.e., "etch stop layer of silicon nitride formed over the first dielectric layer" and "etch stop layer having a dielectric constant below 5.5."

a. "etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core"

Petitioner contends that Watatani describes and depicts etching stopper film 12 of silicon nitride

formed over first conductor core 10 and the underlying dielectric layer. Pet. 35, 47 (citing Ex. 1005, 2:5–7, Figs. 1A–1F).

Patent Owner argues that Watatani's insulation film (i.e., first dielectric layer) is between substrate 1 and lower interconnection pattern 10, which suggests that "when the etching stopper film 12 is formed on the interconnection pattern 10, it cannot be formed over the insulation film." PO Resp. 35.

We have considered Patent Owner's argument, but are persuaded that Petitioner has met its burden of proof for two alternative reasons advanced by Petitioner. Pet. 35, 47; Pet. Reply 2–5.

First, Petitioner persuades us that its contention is based on the broadest reasonable interpretation of the term "over" and that Patent Owner's argument is based on an unduly narrow construction of that term. Pet. Reply 3–4.

Petitioner relies on the following disclosure in Watatani:

> Referring to FIG. lA, a substrate 1 of Si carries thereon a lower interconnection pattern 10 of a conductive material such as Cu, with an insulation film (not illustrated) interposed between the Si substrate 1 and the lower interconnection pattern 10. Further, a first etching stopper film 12 of SiN is formed on the lower interconnection pattern 10 . . . .

Ex. 1005, 2:1–6; Pet. 35, 47; *see also* Ex. 1005, Fig. 1A (showing a sequence of layers from bottom to top: 1, 10, 12, 14, 16, 18). Watatani's etch stop layer 12 is not expressly described as being formed *on* the first dielectric layer (insulation film). Nonetheless,

Petitioner persuades us that the broadest reasonable construction of "over" does not require that the etch stop layer be formed directly "on," or in contact with, the first dielectric layer. Pet. Reply 3–4.

The Specification of the '330 patent uses both terms, "over" and "on," when describing the relationship between various layers. *See, e.g.*, Ex. 1001, 3:51–54 ("[a] dielectric layer is on the semiconductor substrate" and "an etch stop layer [is] over the first dielectric layer and conductor core"). Claims 1 and 6, however, recite an "etch stop layer of silicon nitride formed *over* the first dielectric layer and the first conductor core" (emphasis added), not an etch stop layer formed *on* the first dielectric layer. Patent Owner does not direct us to any intrinsic evidence supporting an express definition or disclaimer that would restrict the meaning of "over" to require direct contact between the etch stop layer and the first dielectric layer. Petitioner, on the other hand, directs us to a description in the Specification where the term "over" is used to describe layers that are not necessarily in direct contact with underlying layers. Pet. Reply 4 (quoting Ex. 1001, 3:4–9 ("The capping layer may be an etch stop layer and may be processed farther for placement of additional levels of channels and vias over it.")). Accordingly, Petitioner persuades us that the term "over," as used in the '330 patent, is broad enough to encompass a structure in which the etch stop layer is formed over the first dielectric layer, with a first conductor core (lower interconnection pattern 10) between the etch stop layer and the first dielectric layer, as Patent Owner acknowledges is disclosed by Watatani. PO Resp. 35.

Petitioner also persuades us that Watatani

teaches or suggests an "etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core," even under Patent Owner's narrow construction of the term "over." Pet. Reply 4 (citing Ex. 1003 ¶¶ 22–35; Ex. 1005, 2:1–5; Ex. 1007,[9] 1 (Fig. 1)).

Watatani discloses that silicon nitride etch stop layer 12 is formed on lower interconnection pattern 10. Ex. 1005, 2:5–6. Watatani's interconnection pattern 10 is a *pattern* of conductive material, not a continuous layer of conductive material. According to Watatani, when the conductive material is copper, such an interconnection pattern is generally formed by a dual damascene process in which a pattern of interconnection grooves and contact holes is formed in an insulation film followed by deposition of a copper layer, which fills the interconnection grooves and contact holes. *Id.* at 1:34–43; *see also* Ex. 1003 ¶ 28 (describing "damascene" technique for copper metallization). The damascene process produces a pattern in which copper is "inlaid" into interconnection grooves and contact holes that have been etched into an insulating film. Ex. 1003 ¶ 28; Ex. 1005, 1:34–43; Ex. 1007, 1 (Figure 1 showing dual damascene process, including step 1: SiN deposition on copper interconnect (Metal 1) pattern).

The layer identified by reference numeral 10 in Watatani Figures 1A– 1F is described as a "Cu interconnection pattern 10," which means the layer comprises a pattern of copper conductors inlaid within an insulating film. Ex. 1003 ¶¶ 27, 28; Ex.

[9] Robert L. Jackson et al., *Processing and Integration of Copper Interconnects*, Solid State Technology, March 1998, pages 49–50, 54, 56, 59 ("SST 1998").

1005, 1:34–43, 2:1–5; *see also* PO Resp. 39 (illustrating "typical" damascene structure in which parallel conductors are separated by insulating material "in the same metal level"). Watatani discloses that silicon nitride etch stop layer 12 is formed "on" interconnection pattern 10, i.e., *on both the conductors and the insulation film of the interconnection pattern*. Ex. 1005, 2:5–6.

Accordingly, Petitioner has shown by a preponderance of the evidence that Watatani discloses an "etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core," as recited in claims 1 and 6, even if the term "over" is construed to mean "on," as Patent Owner implicitly contends. PO Resp. 35.

b. "etch stop layer having a dielectric constant below 5.5"

There is no dispute that Tanaka I discloses a silicon nitride etch stop layer having a dielectric constant below 5.5. Ex. 1006, 1-1 (disclosing "[n]ew low-k SiN film, with permittivity of 5.4" as an etch stop layer for copper damascene interconnects); Pet. 35–36, 48, 51; PO Resp. 28. Dr. Bottoms testifies that "[p]ermittivity as used in Tanaka I means relative permittivity and is synonymous with dielectric constant." Ex. 2001 ¶ 98; *see also* Ex. 1003, 19 n.2 (explaining that the dielectric constant of a material is sometimes referred to as its permittivity and is represented by the letter "k").

There is also no dispute that Watatani discloses a conventional dual damascene structure having silicon nitride etch stop layers. Ex. 1005, 2:5–6 ("a first etching stopper film 12 of SiN"); *id.* at 2:9–11 ("a second etching stopper film 16 of SiN"); *id.* at Figs.

1A–1F (illustrating a conventional dual damascene process, including silicon nitride etch stop layers 12 and 16); Pet. 35, 47, 50; PO Resp. 20.

The parties dispute whether Petitioner has established a motivation and a reasonable expectation of success for the combination of Watatani's conventional dual damascene interconnect structure and Tanaka I's low dielectric constant silicon nitride etch stop layer. For the reasons that follow, we are persuaded that Petitioner has met its burden of proof in this regard. Pet. 13–15, 36, 48–49, 51–52, 56–60.

Petitioner relies on the testimony of Dr. Fair that "[a] person of ordinary skill in the art would have been motivated to use Tanaka's low-k silicon nitride etch stop layer instead of the conventional silicon nitride etch stop layer in the dual damascene structure of Watatani in order to reduce the problem of stray capacitance discussed in both Watatani and Tanaka." Ex. 1003 ¶ 95; *see also id.* ¶ 152 (same); Pet. 36, 48–49, 51–52. We find that Dr. Fair's testimony is credible and supported by the express teachings of Watatani and Tanaka I. Watatani acknowledges the problem of stray capacitance in conventional multilayer interconnect structures and discloses substituting a low dielectric constant insulation film for a conventional insulation film having a large dielectric constant as a solution to the stray capacitance problem. Ex. 1005, 1:23–33, 2:54–64. Tanaka I teaches a similar solution to the same problem, namely, using a "low-k SiN film" as an etch stop layer in an interconnect structure formed by a conventional copper damascene process. Ex. 1006, 1-1, Fig. 1. These disclosures of Watatani and Tanaka I support Dr. Fair's testimony that a POSA would

have been motivated to use Tanaka's low-k silicon nitride etch stop layer in Watatani's conventional dual damascene structure in order to address the problem of stray capacitance. Ex. 1003 ¶¶ 95, 152.

Petitioner relies on the undisputed testimony of Dr. Fair that a POSA "knew long before the filing date of the 330 Patent that one way to reduce the capacitance between two metal lines, and improve interconnect performance, is to reduce the dielectric constant of the materials between those lines." Ex. 1003 ¶ 42; Pet. 13–14. We find that Dr. Fair's testimony is credible and supported by the mathematical formula he provides for calculating the capacitance between two parallel metal plates. Ex. 1003 ¶ 42 (capacitance can be represented by the formula: $C = k\varepsilon_0 A/d$, where k is the dielectric constant of the material between the plates). This equation shows that capacitance is directly proportional to the dielectric constant of the material between the plates. Dr. Bottoms agrees that "capacitance is directly proportional to the area of the conductors and to the relative permittivity or dielectric constant of the dielectric material between the conductors of the capacitor." Ex. 2008 ¶ 37. Dr. Bottoms quotes Dr. Fair's testimony, relying on the same capacitance equation to show "what one of ordinary skill in the art would expect." *Id.* ¶ 153. The known relationship between capacitance and dielectric constant reinforces that a POSA would have been motivated to use a low dielectric constant etch stop layer as a way to reduce stray capacitance between adjacent conductors.

We also credit Dr. Fair's testimony that "a person of ordinary skill in the art would have had a reasonable expectation of success in using Tanaka's

low-k silicon nitride etch stop layers in place of Watatani's conventional silicon nitride etch stop layers in Watatani's conventional dual damascene structure." Ex. 1003 ¶ 153; *see* Pet. 36, 48–49, 51–52, 59. Dr. Fair's testimony is supported by the express disclosures of Tanaka I and Watatani. Tanaka I's low-k silicon nitride film is used for the same purpose as the silicon nitride film in Watatani, namely, as an etch stop layer in a conventional dual damascene copper interconnect structure that uses a silicon oxide insulation film. Ex. 1005, 2:5–6 ("a first etching stopper film 12 of SiN"); *id.* at 2:10–11 ("second etching stopper film 16 of SiN"); *id.* at Figs. 1A–1F (illustrating conventional dual damascene process of forming a multilayer interconnect structure that uses an SiO_2 interlayer insulation film); Ex. 1006, 1-1, Fig. 1 (disclosing new low-k SiN film as the etch stop layer for conventional Cu damascene interconnects with an SiO_2 insulating layer). We find Petitioner's combination would have had a reasonable expectation of success because Tanaka I teaches an improvement to the same type of prior art device described by Watatani as needing improvement—a conventional dual damascene interconnect structure. *In re Inland Steel Co.*, 265 F.3d 1354, 1364 (Fed. Cir. 2001) ("[T]he strength of the correlation between the references gives rise to a reasonable expectation of success from combining them.").

Petitioner directs us to express disclosures in Tanaka I that support a finding that Petitioner's proposed combination would have had a reasonable expectation of success. For example, Petitioner relies on Tanaka I's disclosure: "New low-k SiN film, with a permittivity of 5.4 and high immunity for Cu

diffusion and oxidation, has been *successfully developed*." Ex. 1006, 1-1, 1-2 (emphasis added); Pet. Reply 10. Petitioner also relies on Tanaka I's conclusion that the low-k film, with a permittivity of 5.4, "should be the solution to realize Cu damascene interconnects for high performance VLSIs." Ex. 1006, 1-1, 1-2; Pet. 59. As noted by Petitioner, Tanaka I summarizes the results of various experiments by stating "superior process results and film properties" for its low-k silicon nitride layer are presented. Ex. 1006, 1-1; Pet. 58. From the results of etch rate selectivity tests, for example, Tanaka I concludes that the disclosed low-k silicon nitride film has "enough ability for etching stopper." Ex. 1006, 1-2; *see* Pet. Reply 16. Petitioner persuades us that these disclosures would have provided a POSA with a reasonable degree of confidence that Tanaka I's low-k silicon nitride film would function as an etch stop in Watatani's conventional dual damascene interconnect structure. Pet. 58–59; Pet. Reply 10–11, 15–17.

We now turn to Patent Owner's arguments contesting motivation to combine and a reasonable expectation of success.

Patent Owner begins by focusing on Watatani, arguing it "does not teach that silicon nitride etch stops are a source of stray capacitance" and "offers no motivation related to etch stop layers having a low dielectric constant." PO Resp. 36, 37. We have considered Patent Owner's argument, but are nevertheless persuaded by Petitioner's reliance on Watatani as evidence of a motivation to combine. As Petitioner persuasively argues, Watatani is concerned with the same problem addressed by Tanaka I and the '330 patent, namely, the problem of

stray capacitance in conventional dual damascene interconnect structures. Pet. 56–57; Ex. 1001, 3:32–42; Ex. 1005, 1:23–33; Ex. 1006, 1-1. Watatani recognizes the relationship between stray capacitance and the dielectric constant of layers used to make a multilayer interconnect, and addresses the problem of stray capacitance in a manner similar to Tanaka I and the '330 patent, namely, by replacing a high dielectric constant film with a low dielectric constant film. Ex. 1005, 2:54–64. It is true that Watatani's solution pertains to a different material layer than either Tanaka I or the '330 patent—the silicon oxide interlayer insulation film, rather than the silicon nitride etch stop layer. *Id.* But Watatani nevertheless supports and is fully consistent with Petitioner's contention that a POSA would have been motivated to address the problem of stray capacitance by replacing a high dielectric constant material with a lower dielectric constant material, such as by replacing a high dielectric constant etch stop layer with a low dielectric constant etch stop layer.

Next, Patent Owner argues there is no evidence that a POSA would have been motivated to adopt Tanaka I's solution either "in lieu of" or "in addition to" Watatani's solution, which uses a low dielectric constant organic insulation film to reduce parasitic capacitance. PO Resp. 37–38, 44. Patent Owner's argument misconstrues Petitioner's obviousness contention, which is based on Watatani's conventional dual damascene interconnect structure that uses conventional inorganic insulating films, not Watatani's proposed improvements to that conventional structure that use lower dielectric constant organic insulating films. *See, e.g.*, Pet. 35

(referencing the conventional dual damascene structure shown in Watatani Figures 1A– 1F). *See In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) ("The use of patents as references is not limited to what the patentees describe as their own inventions." (internal quotations omitted)).

Patent Owner's argument also misconstrues Petitioner's burden. Petitioner's obviousness case is not undermined by Watatani's disclosure of alternative techniques for reducing stray capacitance. *See* Pet. 59–60 (discussing Watatani's disclosure of organic insulating layers). To prove its case, Petitioner needs to show that a POSA "would have seen a benefit" from improving Watatani's conventional dual damascene interconnect structure with Tanaka I's low-k silicon nitride etch stop layer. *See KSR*, 550 U.S. at 424 (in assessing obviousness, the "proper question" is whether a person of ordinary skill in the art "would have seen a benefit" to upgrading a known device with another feature known in the art in the manner claimed by patentee).

Obviousness may be shown even if Petitioner's combination of Watatani and Tanaka I would have been less effective at reducing stray capacitance than Watatani's embodiments having an organic insulation film. *See, e.g.*, *Slot Speaker Techs., Inc. v. Apple Inc.*, 680 F. App'x 932, 940 (Fed. Cir. 2017) ("It is irrelevant whether Tomonori and Sadaie together would be less effective than Sadaie alone at avoiding the absorption of certain low frequencies."). Petitioner's burden is to show that the claimed invention would have been obvious to a POSA at the time of the invention, not that it was the best option available to a POSA. *In re Mouttet*, 686 F.3d 1322,

1334 (Fed. Cir. 2012) ("[J]ust because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.").

Next, Patent Owner argues that "reducing the dielectric constant of etch stop layers . . . might have limited impact" on reducing parasitic capacitance, and reducing the dielectric constant of other layers "might outweigh the effect of reducing the dielectric constant of etch stop layers." PO Resp. 38. According to Patent Owner, the dielectric constant of etch stop layers has "little or no effect" on capacitive coupling, which Patent Owner asserts is more significant than stacked capacitance as a source of parasitic capacitance. *Id.* at 38–41 (citing Ex. 2008 ¶¶ 124, 125, 127; Ex. 2009, 65:12–66:8; Ex. 2010,[10] 3, Figs. 2, 5; Ex. 2011,[11] 3, Fig. 8).

Again, Patent Owner's argument misconstrues Petitioner's burden, which does not require proof that the benefit of Petitioner's combination outweighs the benefit of other available options, such as reducing the dielectric constant of other layers. *Slot Speaker*, 680 F. App'x at 940; *Mouttet*, 686 F.3d at 1334. We agree with Petitioner that Patent Owner's argument is contrary to the teachings of Tanaka I, which states that low-k silicon nitride etch stop layer "should be the solution" to the "parasitic

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[10] M. Igarashi, et al., *The Best Combination of Aluminum and Copper Interconnects for a High Performance 0.18μ CMOS Logic Device*, IEEE International Electron Devices Meeting, 829–32 (1998) ("Igarashi").

[11] G. Lecarval, et al., *Advanced Interconnect Scheme Analysis: Real Impact of Technological Improvements*, IEEE International Electron Devices Meeting, 837–40 (1998) ("Lecarval").

capacitance" problem caused by the "high permittivity of [conventional] SiN." Ex. 1006, 1-1; Pet. Reply 5–6.

Although Patent Owner relies on Igarashi (Ex. 2010) and Lecarval (Ex. 2011) (*see* PO Resp. 38–41; Ex. 2008 ¶¶ 125–127), Petitioner persuades us that these references do not support Patent Owner's position. Pet. Reply 7. As noted by Petitioner, Tanaka I cites Igarashi and Lecarval as support for Tanaka I's statement that the "high permittivity of [conventional] SiN" contributes to the performance degradation of copper damascene structures due to "parasitic capacitance." Ex. 1006, 1; Pet. Reply 7. We give greater weight to Tanaka I's 1999 interpretation of Igarashi and Lecarval than to Dr. Bottoms' *post hoc* opinion that reducing the dielectric constant of etch stop layers "might have limited impact" on parasitic capacitance. Ex. 2008 ¶ 124.

Moreover, Petitioner directs us to disclosures in Igarashi and Lecarval that contradict Patent Owner's argument. Pet. Reply 6–7 (discussing Ex. 2010, 1-2; Ex. 2011, Fig. 8). For example, Igarashi teaches "it is not desirable for the interconnects to contain such a high Si_3N_4 [silicon nitride] film with a 'high-k' dielectric, because the effective dielectric constant clearly increases." Ex. 2010, 1-2. Similarly, based on the comparison in Figure 8, Lecarval concludes that "[f]or damascene [structures], the low-k material slightly improves" the cross-talk sensitivity. Ex. 2011, 3-1.[12] Lecarval characterizes

[12] Lecarval's conclusion is based on Figure 8, which compares cross-talk sensitivity, X, as a function of metallization layer thickness for three different structures at two different pitches (0.4 μm and 0.6 μm): (1) a non- damascene structure with an Al metallization layer and a low-k dielectric; (2) a "Cu SiO_2"

the effect of low dielectric constant materials as an improvement, even though "the impact of the materials remains low." *Id.*

Next, Patent Owner argues there is no evidence "that replacing conventional silicon nitride etch stops would cause a meaningful reduction in parasitic capacitance, relative to Watatani's low dielectric constant spin- on glass damascene structure." PO Resp. 42. Again, Patent Owner's argument misconstrues Petitioner's burden, which does not require proof that Petitioner's combination of Watatani and Tanaka I is an improvement relative to Watatani's embodiments that use organic spin-on glass ("SOG") film. *Slot Speaker*, 680 F. App'x at 940; *Mouttet*, 686 F.3d at 1334. *See* Ex. 1005, 3:4–14, 5:61–66, 6:1–3 (disclosing SOG embodiments).

Next, Patent Owner identifies various parameters, such as etch stop layer thickness, that are not disclosed by Watatani and asserts, because these parameters are unknown, a POSA "would have no basis to conclude" that stray capacitance would be reduced by modifying Watatani's device to incorporate Tanaka I's low dielectric constant silicon nitride etch stop layer. PO Resp. 42–44 (citing Ex. 2008 ¶ 130; Ex. 1013,[13] Fig. 17). We disagree. Patent

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damascene structure having etch stop layers with a permittivity of 7 and thicknesses of 0.04 μm and 0.12 μm and a dielectric layer with a permittivity of 4; and (3) a "Cu low k" damascene structure having etch stop layers with a permittivity of 4 and thicknesses of 0.04 μm and 0.04 μm and a dielectric layer with a permittivity of 3. Ex. 2011, 1-2, 2-1, 3-1 (Table 1, Figs. 3 and 8).

[13] Masayuki Tanaka, et al, *Film Properties of Low-k Silicon Nitride Films Formed by Hexachlorodisilane and Ammonia*, Journal of The Electrochemical Society, 147 (6) 2284–89 (2000) ("Tanaka II").

Owner's argument does not adequately account for the express teachings of Watatani and Tanaka I and the known relationship between dielectric constant and capacitance, which Petitioner has persuasively relied upon to show that a POSA would have been motivated to use a low dielectric constant silicon nitride etch stop layer to reduce stray capacitance. *See* pages 20–21, *supra.*

Next, Patent Owner argues that replacing Watatani's conventional silicon nitride etch stop layer with Tanaka I's low dielectric constant etch stop layer "may require increasing the thickness of the etch stop layer by an amount that would cause an overall increase in stray capacitance." PO Resp. 43 (citing Ex. 2008 ¶ 130; Ex. 2009, 70:6–71:12). We find Patent Owner's argument is speculative and not supported by the record as a whole. Although Patent Owner and Dr. Bottoms make vague references to etch selectivity (PO Resp. 42; Ex. 2008 ¶ 129), on this record, it would be entirely speculative to find that a thicker layer would be required for purposes of etch selectivity. We are persuaded by Petitioner's arguments and Dr. Fair's testimony directing us to disclosures in Tanaka I and Tanaka II that use of low-k silicon nitride would have permitted a thinner-than-conventional etch stop layer. Pet. Reply 7–8; Ex. 1017 ¶ 18 (both quoting Ex. 1006, 1; Ex. 1013, 6).

Next, Patent Owner asserts that the presence of chlorine in Tanaka I's HCD-SiN material would have driven a POSA away from using Tanaka I's approach because chlorine was known to corrode copper interconnects. PO Resp. 44 (citing Ex. 2008 ¶¶ 101, 104). We are persuaded by Petitioner's response to Patent Owner's assertion, which relies on Dr. Fair's detailed analysis, supported by citations to Tanaka I,

explaining why a POSA would not have been concerned about the presence of chlorine in Tanaka I's silicon nitride etch stop material. Pet. Reply 8–9; Ex. 1017 ¶ 19 (citing and quoting Ex. 1006, title, 1-2, Fig. 8). For example, Petitioner and Dr. Fair rely on Tanaka I's tests showing stability of chlorine in low-k films. Pet. Reply 8; Ex. 1017 ¶ 19; Ex. 1006, 1-2. In contrast, Dr. Bottoms' opinions regarding chlorine corrosion of copper interconnects is unsupported by citations to Tanaka I or other evidence. Ex. 2008 ¶¶ 101, 104. In fact, Dr. Bottoms admits "*[t]here is no data* on . . . corrosion of Cu in the metallization." *Id.* ¶ 139 (emphasis added). Patent Owner had the opportunity to cross-examine Dr. Fair's reply testimony and submit observations or to request a sur-reply on this topic, but declined to do so. Under these circumstances, we find that Dr. Fair's testimony regarding chlorine corrosion of copper interconnects to be more credible than Dr. Bottoms' testimony on this topic.

Turning to the issue of reasonable expectation of success, Patent Owner argues that Tanaka I provides "insufficient information" to suggest that Tanaka I's HCD-SiN films "would work as etch stop layers in Watatani's process or that such etch stop layers could be made thin enough in Watatani's process to ultimately lower the device capacitance." PO Resp. 45 (citing Ex. 2008 ¶ 132). Patent Owner asserts that Tanaka I "omits critical characteristics of the HCD-SiN material, making its suitability as an etch stop speculative at best." *Id.*

We agree with Petitioner that Patent Owner's arguments do not accurately characterize Tanaka I, which states that the HCD-SiN film "has been successfully developed" and discloses tests designed

to show that HCD-SiN will work as an etch stop layer in copper damascene metallization structures like Watatani's. Pet. Reply 10–11; Ex. 1006, 1, Fig. 1; Ex. 1017 ¶¶ 22, 23. In our view, Patent Owner's arguments demand more of the prior art than is provided by the sparse disclosure of the '330 patent. *See* Pet. 19 ("the 330 Patent sets forth few details on how to accomplish the reduction [in dielectric constant] or implement the methods"). Most of the information Patent Owner contends is missing from Tanaka I is not disclosed by the '330 patent. For example, the '330 patent does not disclose etch chemistries, etch selectivity, or the thickness of the dielectric layers being etched. *Cf.* PO Resp. 48 (listing etch chemistry and relative thickness of the materials as factors affecting suitability as an etch stop); *id.* at 49 (asserting that Tanaka I does not disclose etch selectivity between SiO_2 and HCD-SiN). Nor does the '330 patent disclose any information regarding the barrier property of silicon nitride etch stop layers. *Cf.* PO Resp. 50–52 (asserting that barrier property is a necessary characteristic of an etch stop and the disclosure of Tanaka I is deficient in this regard). Tanaka I provides at least as much, if not more, information than the '330 patent regarding suitability of low dielectric constant silicon nitride as an etch stop layer. Ex. 1006, 1-2, 2-2, Fig. 6 ("Selectivity of RIE etching rate versus TEOS"). The '330 patent's sparse disclosure, as compared with Tanaka I's more detailed disclosure, persuades us that Tanaka I's disclosure is sufficient to provide a reasonable expectation of success of achieving the claimed invention. *See Trustees of Columbia Univ. in City of New York v. Illumina, Inc.*, 620 F. App'x 916, 929 (Fed. Cir. 2015) (relying on disclosure of

challenged patent as substantial evidence sufficient to support PTAB's finding of a reasonable expectation of success in combining prior art references and synthesizing the claimed nucleotide).

Patent Owner faults Petitioner for not presenting evidence of a commercial product that uses Tanaka I's HCD-SiN as an etch stop layer. PO Resp. 47. We agree with Petitioner, however, that commercial success of the prior art is not a requirement for proof of obviousness. Pet. Reply 12. *In re Wright*, 569 F.2d 1124, 1128 (C.C.P.A. 1976) (obviousness should be measured against the nearest prior art, even if it is not "the commercial standard"). Patent Owner argues that later research "likely served as a deterrent that prevented adoption" of Tanaka I's HCD-SiN material. PO Resp. 47 (citing Ex. 2008 ¶ 134; Ex. 2012,[14] 2, 4, Fig. 7; Ex. 2013,[15] 1)). As noted by Petitioner, however, both references relied upon by Patent Owner were published after the filing date of the '330 patent, which means they are not relevant to determining whether there would have been a reasonable expectation of success. Pet. Reply 12 n.4. *Bristol-Myers Squibb Co. v. Teva Pharm., Inc.*, 752 F.3d 967, 976 (Fed. Cir. 2014) ("the skilled artisan's reasonable expectation of success is measured 'as of the date of the invention'" (quoting *Amgen Inc. v.*

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[14] Masayuki Tanaka et al., *Suppression of SiN-Induced Boron Penetration by Using SiH-Free Silicon Nitride Films Formed by Tetraschlorosilane and Ammonia*, 49 IEEE Transactions in Electron Devices 1526–31 (2002) ("Tanaka III").

[15] N. Mise, et al., *Suppression of Gate-Edge Metamorphoses of Metal/High- k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact on Scaled MOSFETs*, Extended Abstracts of the 2007 Int'l Conf. on Solid State Devices and Materials, Tsukuba, 724–35 (2007) ("Mise").

Hoffman-La Roche, 580 F.3d 1340, 1362 (Fed. Cir. 2009)). Furthermore, neither Patent Owner nor its expert explains how the later research (Exs. 2012, 2013) relates to a reasonable expectation of success for HCD-SiN film as an etch stop layer in copper damascene interconnect structures.

Relying on Dr. Fair's testimony about a need for further investigation, Patent Owner argues that a POSA would have recognized "a degree of uncertainty" when using Tanaka I's HCD-SiN material as an etch stop layer. PO Resp. 49 (citing Ex. 2009, 55:6–16, 77:22–78:1, 83:12–84:5). But Patent Owner does not argue that undue experimentation would be required, agreeing with Dr. Fair that any necessary experimentation would be "standard." *Id.* Petitioner directs us to the testimony of Dr. Fair and disclosures in Tanaka I, which persuade us that implementing Tanaka I's HCD-SiN material as an etch stop layer would have been within the level of skill in the art at the relevant time. Pet. Reply 14; Ex. 1003, ¶ 35; Ex. 1006, 1-1; Ex. 2009, 55:6–16, 77:9–78:10, 78:19–79:22. Moreover, Patent Owner's argument regarding "a degree of uncertainty" is inconsistent with the legal standard for a reasonable expectation of success. *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) ("certainty of success" is not required).

In the same vein, Patent Owner relies on Tanaka I's data regarding etch selectivity and Auger profiles to argue that a POSA would have recognized a "risk of over etching" and "doubted" the barrier ability and long-term stability of Tanaka I's HCD-SiN film. PO Resp. 50–52 (citing Ex. 2008 ¶¶ 138, 139); *see also* PO Sur-Reply (data in Tanaka I "raise[s] questions

that would need investigation”). We agree with Petitioner that Patent Owner’s arguments are contradicted by the express disclosures of Tanaka I, including its statements that HCD-SiN “is concluded to have enough ability for etching stopper,” has the “same RIE etching resistance as conventional LPCVD SiN,” and has “higher barrier ability for Cu diffusion than plasma-SiN.” Pet. Reply 15–16; Ex. 1006, 1-1, 1-2. Moreover, Patent Owner’s arguments regarding “risk,” “doubt[],” and “questions” (PO Resp. 50–52) are inconsistent with the legal standard for a reasonable expectation of success. *In re Kubin*, 561 F.3d 1351, 1360 (Fed. Cir. 2009) (“Obviousness does not require absolute predictability of success . . . all that is required is a reasonable expectation of success.” (citing *In re O’Farrell*, 853 F.2d 894, 903–04 (Fed. Cir. 1988))); *Medichem*, 437 F.3d at 1165.

Similarly, Patent Owner argues that the dielectric constant of HCD- SiN material would be affected by the deposition rate and would “likely” be affected by other parameters, such as deposition pressure, temperature, and layer thickness. PO Resp. 52–53 (asserting that “achieving a practical deposition rate . . . would require a corresponding increase in the dielectric constant” (citing Ex. 2008 ¶ 140)); PO Sur-Reply 2 (“Forming an etch stop layer with a dielectric constant of less than 5.5 . . . was uncertain.”). Again, Patent Owner’s arguments are inconsistent with the legal standard for a reasonable expectation of success, which does not require manufacturability at practical rates, nor absolute certainty of success. *In re Kubin*, 561 F.3d at 1360; *Medichem*, 437 F.3d at 1165. Regardless, Petitioner presents credible, unrebutted testimony of Dr. Fair that a POSA would have understood that slower

deposition rates provide advantages over faster rates. Pet. Reply 13; Ex. 1017 ¶ 25.

After considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that a POSA would have been motivated to combine Watatani's conventional dual damascene interconnect structure with Tanaka I's low dielectric constant silicon nitride etch stop layer and would have had a reasonable expectation of success of achieving the claimed subject matter.

Accordingly, we are persuaded Petitioner has established by a preponderance of the evidence that claims 1 and 6 of the '330 patent are unpatentable as obvious in view of Watatani and Tanaka I.

2. Claims 2 and 7

Claim 2 depends from claim 1 and recites "wherein the etch stop layer is a multilayer structure." Ex. 1001, 7:3–4. Claim 7 depends from claim 6 and recites "wherein the via and channel etch stop layers are a multilayer structure." *Id.* at 8:12–13.

Petitioner contends that "Watatani expressly describes an etch stop layer that includes 'three or more layers' of silicon nitride." Pet. 39, 54 (citing Ex. 1005, 7:54–55). Petitioner also contends that it was well known in the prior art to form multilayer silicon nitride films. *Id.* at 15, 20, 39, 54. Petitioner contends that a POSA would have been motivated to use a multilayer approach because it would improve the uniformity of the etch stop film and improve its dielectric properties by avoiding pinholes. *Id.* at 16, 20, 40–41, 55.

In the Institution Decision, we rejected Petitioner's contention that Watatani describes an etch stop layer that includes three or more layers of silicon nitride. Dec. 17–18. Nevertheless, we instituted review on the basis of Petitioner's contentions that multilayer silicon nitride layers were known in the art and that a POSA would have known of the advantages of a multilayer approach and would have been motivated to use that approach in view of its advantages. *Id.* at 18–19. In the Rehearing Decision, we rejected Patent Owner's argument that the Institution Decision introduced a new ground not asserted in the Petition. We stated: "even though SST 1987[16] is necessary to establish *prima facie* obviousness, there is no abuse of discretion or prejudice to Patent Owner because the Petition and the Decision each independently put Patent Owner on notice of the reference and the way in which it is relied upon by Petitioner and the Board." Reh'g Dec. 4.

Patent Owner argues that Watatani does not disclose a multilayer silicon nitride etch stop and that, by relying on SST 1987, the Institution Decision improperly expanded the ground of unpatentability asserted in the Petition. PO Resp. 54–60. In addition, Patent Owner challenges the sufficiency of the evidence to establish motivation and a reasonable expectation of success for forming Tanaka I's HCD-SiN etch stop as a multilayer structure. *Id.* at 60–68.

Patent Owner does not dispute Petitioner's contention that multilayer silicon nitride layers were

[16] *Continuous Process CVD System*, Solid State Technology, October 1987, Ex. 1008 ("SST 1987").

known in the prior art. Pet. 15–16, 20, 39, 54 (citing Ex.1003 ¶¶ 45–47, 105–107; Ex. 1008, 1-1, 2-1, Fig. 2; Ex. 1010[17]). Petitioner directs us to persuasive evidence, including Dr. Fair's testimony that a POSA "would have long known of equipment and techniques to deposit silicon nitride layers using a multilayer deposition technique." Ex. 1003 ¶ 45 (citing Ex. 1008, 1). Dr. Fair relies on SST 1987, which describes the Novellus Concept One Chemical Vapor Deposition (CVD) system. Ex. 1008, 1-1. According to SST 1987, the process chamber of the Concept One has eight stations, seven of which are used for depositing films on a wafer. *Id.* SST 1987 discloses that the Concept One enables "a new approach to chemical vapor deposition, in which every wafer that cycles through the system stops at each of the seven deposition stations to receive one seventh of its preprogrammed film thickness." *Id.* Petitioner's contention is also supported by Wang, which discloses a multilayer silicon nitride deposition method and a multilayer silicon nitride layer. Ex. 1010, title, 11:8–18.

Dr. Bottoms agrees that SST 1987 "discloses depositing SiN films using seven consecutive deposition steps." Ex. 2008 ¶ 163. Dr. Bottoms does not dispute Dr. Fair's testimony that the Concept One tool was widely used in the semiconductor industry in the 1980s and 1990s. Ex. 1003 ¶ 45. In fact, Dr. Bottoms testifies that he is familiar with multi-station deposition systems, including the Novellus Concept One, and managed a group that developed a precursor machine that was "introduced in the early 1980's" and "designed to sputter deposit

[17] Wang et al., US 6,017,791, issued January 25, 2000 ("Wang").

films in a multi-station vacuum chamber." Ex. 2008 ¶ 148 (discussing the Varian 3180).

Petitioner and Dr. Fair direct us to substantial evidence that it was known in the art to use multilayer silicon nitride layers as an etch stop layer in copper damascene interconnect structures. Pet. Sur-Sur-Reply 3; Ex. 1017 ¶ 33; Ex. 1023 (Yota),[18] 1-2. Yota discloses silicon nitride films for use as etch stop layers in copper damascene architectures and compares films deposited by high-density plasma ("HDP") CVD with films deposited by plasma-enhanced CVD ("PECVD"). *Id.*, Title, Abstract. Yota reports the results of experiments in which "[t]he PECVD films were deposited in a six-station deposition system." *Id.* at 1-2. Dr. Fair testifies that "Yota . . . is prior art for the use of multilayer silicon nitride films as etching stoppers." Ex. 1017 ¶ 33.[19]

Petitioner has shown by a preponderance of the evidence that a POSA would have been motivated to use a multilayer approach, as taught by SST 1987, when forming a low dielectric constant silicon nitride etch stop layer, as taught by Tanaka I, and would have had a reasonable expectation of success in

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[18] J. Yota, et al., *Comparison between HDP CVD and PECVD Silicon Nitride for Advanced Interconnect Applications*, Proc. of the IEEE 2000 Int'l Interconnect Tech. Conf. (2000) ("Yota"). Yota was submitted with Petitioner's Reply. Patent Owner requested and received the opportunity to file a sur-reply and declaration testimony responding to Yota. PO Sur- Reply 6–7; Ex. 2014, 2; Ex. 2015 ¶¶ 16–18.

[19] In view of our finding that multilayer silicon nitride etch stop layers were known in the prior art, as evidenced by Dr. Fair's testimony, Dr. Bottoms' testimony, SST 1987, and Yota, it is unnecessary to address Petitioner's contention that Watatani discloses an etch stop layer that includes three or more layers of silicon nitride. Pet. 39, 54; Pet. Reply 19–20.

achieving the subject matter of claims 2 and 7. Pet. 16, 20, 40–41, 55 (citing Ex. 1003 ¶¶ 46, 47, 106–109, 143; Ex. 1008, 2-2; Ex. 1010, 11:8–18); *see also* Ex. 1003 ¶¶ 156, 157. Petitioner's evidence shows two motivations for a multilayer structure: (1) improved film uniformity, and (2) improved dielectric properties by avoiding pinholes. Pet. 40–41. We discuss each of these motivations below:

First, Petitioner presents the undisputed testimony of Dr. Fair establishing that a POSA would have known that forming silicon nitride layers in a multi-layer fashion was advantageous because this approach produced more uniform thin films. Ex. 1003 ¶¶ 46, 106, 108, 143, 156 (citing Ex. 1008, 2-1). Dr. Fair's testimony is supported by 1987 SST, which describes uniformity as an "inherent benefit[]" of a multilayer deposition process using the Novellus Concept One CVD tool. Ex. 1008, 2-1. The article explains: "Within wafer *uniformity is improved* because deposition anomalies at any individual [deposition] station are averaged out, while at the output end wafer-to-wafer variations are significantly reduced because of the overall averaging effect of the process." *Id.* (emphasis added). The undisputed testimony of Dr. Fair further establishes that "[s]uch film uniformity is important in an etch stop layer, as non-uniform thin regions are prone to unintended 'punch through.'" Ex. 1003 ¶ 46. Patent Owner and Dr. Bottoms do not disagree that a POSA "would have been motivated to 'improve the uniformity' of etch stop layers by using the Novellus Concept One system described in the SST 1987 article" to deposit multiple layers of the same material. PO Resp. 63; Ex. 2008 ¶ 149.

Second, Petitioner presents credible testimony of

Dr. Fair establishing that a desire for improved dielectric properties would have motivated the use of a multilayer silicon nitride film. Ex. 1003 ¶¶ 47, 107, 108, 156 (citing Ex. 1010, 11:8–18). According to Dr. Fair, "it was known in the prior art that forming a multilayer silicon nitride layer comprising at least two layers of silicon nitride on which a silicon oxide layer is formed, one could avoid 'pinholes formed completely through the silicon nitride/silicon oxide (NO) layer,' which avoids 'degraded dielectric properties' of the dielectric layers." Ex. 1003 ¶ 47 (quoting Ex. 1010, 11:8–18).

Dr. Fair's testimony is supported by Wang, which discloses forming a multilayer silicon nitride layer by CVD on a silicon oxide layer, which is then thermally oxidized to form a silicon nitride/silicon oxide (NO) layer. Ex. 1010, 10:5–48, 11:8–35, 11:46–56, Fig. 2. Wang discloses an advantage of multilayer deposition as follows:

> [W]hen employing the multilayer silicon nitride layer formed from the first silicon nitride layer 36a and the second silicon nitride layer 36b to subsequently form from the multilayer silicon nitride layer a silicon nitride/silicon oxide (NO) layer through a thermal oxidation method, there is avoided pinholes formed completely through the silicon nitride/silicon oxide (NO) layer, which pinholes would otherwise contribute to degraded dielectric properties of the silicon nitride/ silicon oxide (NO) dielectric layer . . .

Id. at 11:8–18. Although Wang does not relate to etch stop layers, Dr. Fair testifies that pinholes are undesirable in etch stop layers, explaining that pinholes can "function as localized defects that can

alter the etch rate at individual points of an etch stop layer." Ex. 1003 ¶ 156. Dr. Fair's testimony is consistent with SST 1998, which shows that the absence of pinholes is important for silicon nitride etch stop layers for copper damascene interconnect structures. SST 1998 teaches that silicon nitride etch stop layers must be "pinhole-free so that its diffusion barrier properties are not compromised." Ex. 1007, 2-1.

Turning to the issue of reasonable expectation of success, Petitioner directs us to the following testimony of Dr. Fair, which we find persuasive:

> A person of ordinary skill in the art would also have had a reasonable expectation of success in depositing Tanaka's low-k silicon nitride film as a series of multiple layers in the prior art dual damascene structure of Watatani, because devices designed to create multilayer etch stops were available in the prior art, and the use of a multilayer silicon nitride etch stop for this purpose was widely known in the prior art.

Ex. 1003 ¶ 109 (citing Ex. 1010, 11:8–18); *see* Pet. 41; *see also* Ex. 1003 ¶ 157 ("Because the multilayer deposition technique and its benefits was widely known in the prior art, and because the Novellus Concept One was broadly available commercially, a person of ordinary skill in the art would have had a reasonable expectation of success in depositing Tanaka's low-k silicon nitride film as a series of multiple layers in the prior art dual damascene structure of Watatani." (citing Ex. 1008, 2, Fig. 2)). Dr. Fair's testimony is supported by SST 1987, which discloses a seven-station CVD system for sequentially depositing multiple layers of a dielectric

film, such as silicon nitride. Ex. 1008, 1-1. Dr. Fair's testimony is consistent with Yota, which discloses depositing a silicon nitride etch stop layer using a six- station sequential deposition system. Ex. 1023, 1-2; *see* Pet. Sur-Sur-Reply 3 (citing Ex. 1023, 1-2).

We are also persuaded by Dr. Fair's testimony that "a person of ordinary skill in the art would have had a reasonable expectation of success at keeping the dielectric constant below 5.5 when employing a multilayer silicon nitride etch stop." Ex. 1017 ¶ 34; *see* Pet. Reply 26 (citing Ex. 1017 ¶ 34); *see also* Pet. Sur-Sur-Reply 4 (discussing Dr. Fair's testimony regarding dielectric constant of multilayer silicon nitride film). Dr. Fair provides a credible technical explanation for his opinion: "when stacking very thin layers to form a multilayer film, the dielectric constant can remain lower than a single layer film of the same overall thickness because of the interactions of the interfacial layers and the bulk properties of the thin layers." *Id.* ¶ 35. As further discussed below, Dr. Bottoms provides no credible rebuttal to Dr. Fair's opinion, which is consistent with Dr. Bottoms' testimony regarding a POSA's understanding about the relationship between multiple thin layers, density, and dielectric constant. Ex. 2008 ¶ 40.

We turn now to Patent Owner's arguments, starting with the procedural challenge to our Institution Decision. PO Resp. 56–60.[20] Patent

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[20] Because we do not rely on Watatani to teach a multilayer silicon nitride etch stop layer, we do not need to address Patent Owner's argument that this feature is not disclosed by Watatani (PO Resp. 54–56) or Patent Owner's related arguments regarding lack of motivation (*id.* at 61, 63) and defeating the purpose of Watatani's structure (*id.* at 67–68).

Owner is correct that the Petition controls the scope of an *inter partes* review. PO Resp. 56 (citing *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348 (2018) and 35 U.S.C. § 311(a)); *see also Sirona Dental Sys. GmbH v. Institut Straumann AG*, 892 F.3d 1349, 1356 (Fed. Cir. 2018) ("It would . . . not be proper for the Board to deviate from the grounds in the petition and raise its own obviousness theory."). We have complied with that requirement. Our Institution Decision (and this final decision) rely on SST 1987 in the *same way* as it was relied upon in the Petition: as evidence that multilayer silicon nitride layers were known in the prior art. Dec. 18–19. We disagree with Patent Owner's assertion that "Petitioner relies exclusively on teachings of Watatani to disclose the multilayer silicon nitride etch stop structure required by claims 2 and 7." PO Resp. 57. The Petition plainly relies on SST 1987 (in addition to Watatani) for this teaching. Pet. 15–16, 20, 39–41, 53–55. Petitioner's arguments regarding motivation and reasonable expectation of success apply to "the multilayer approach," including the multilayer deposition technique of SST 1987. Pet. 40–41, 55. We agree with Petitioner that the statements in the Petition regarding the benefits of a multilayer silicon nitride etch stop "are clearly not in reference to Watatani's specific approach (to the extent it is different), but to the general understanding in the art of using a multilayer etch stop as evidenced by, e.g., the SST 1987 reference." Pet. Reply 23 (citing Pet. 40–41). The fact that SST 1987 was not listed alongside Watatani and Tanaka I in the summary of the ground (Pet. 4) or section heading (Pet. 29) does not mean it was not part of the ground of unpatentability asserted in the Petition. Patent Owner's counterargument elevates

form over substance.

Patent Owner relies on *In re NuVasive, Inc.*, 841 F.3d 966 (Fed. Cir. 2016)—*see* PO Resp. 60—but that case is distinguishable. In *NuVasive*, the court held that patent owner was not given an adequate notice and opportunity to respond to the Board's assertions of fact regarding a prior art reference. 841 F.3d at 970–73 (citing the Administrative Procedure Act ("APA"), 5 U.S.C. § 706). The reference in *NuVasive* was relied upon for a particular claim element for the first time in petitioner's reply, and patent owner was not given an opportunity to file a sur-reply or even to address the point in the oral hearing. *Id.* at 973. In contrast to *NuVasive*, Patent Owner in this case was given notice and an opportunity to respond to Petitioner's and the Board's assertions of fact regarding SST 1987. Notice was given in the Petition, the Institution Decision, and the Rehearing Decision, all of which expressly rely upon SST 1987 to teach multilayer silicon nitride layers, and all of which were filed before the Patent Owner Response. Pet. 15–16, 20, 39–41, 53–55; Dec. 18–19; Reh'g Dec. 3–4. Moreover, Patent Owner concedes that it had adequate notice and an opportunity to respond to Petitioner's arguments based on SST 1987 and the Novellus Concept One CVD system. Tr. 25:15–24. Accordingly, there is no APA concern here, and *NuVasive* is not applicable.

Next, Patent Owner challenges the sufficiency of Petitioner's evidence of motivation and reasonable expectation of success, arguing "Wang does not provide any certainty that a multilayered structure would eliminate pinholes in the claimed device." PO Resp. 62. Patent Owner's argument is inconsistent with the legal standard for a reasonable expectation

of success, which does not require certainty of success. *In re Kubin*, 561 F.3d at 1360; *Medichem*, 437 F.3d at 1165. In addition, we agree with Petitioner that Patent Owner's argument is contrary to the express disclosures of Wang and Dr. Fair's testimony that the benefit of reducing pinholes was well known in the art. Pet. Reply 24 (citing Ex. 1010, 11:8–25; Ex. 1003 ¶¶ 106–108).

Next, Patent Owner argues that Wang's multilayer deposition method requires a purge step that is not described by SST 1987 and, "given this difference in the process," the multilayer structure of the Novellus Concept One might not eliminate pinholes. PO Resp. 62. We agree with Petitioner that the express teachings of one reference do not need to be reiterated by all references in order to show motivation. Pet. Reply 24–25. Even if the advantages described by Wang and SST 1987 were mutually exclusive, they each independently provide a motivation for a multilayer structure. Ex. 1008, 2-1 (improved uniformity); Ex. 1010, 11:8–18 (avoiding pinholes).

Next, Patent Owner argues that Petitioner does not establish that the dielectric constant of Tanaka I's HCD-SiN material would remain below 5.5 if it was deposited as a series of multiple layers. PO Resp. 64. As support for this argument, Patent Owner directs us to Dr. Fair's admittedly erroneous testimony regarding Figure 17 of Tanaka II and what it shows about the relationship between thickness and dielectric constant for silicon nitride layers. *Id.* at 64–65 (citing Ex. 1003 ¶¶ 44, 55, 109, 156; Ex. 1013, 5, Fig. 17; Ex. 2009, 16:7–25, 17:11–18:7, 19:6–21, 21:20–22:18). In our view, Dr. Fair's admitted error does not support Patent Owner's

argument, nor does it warrant discrediting Dr. Fair's testimony about reasonable expectation of success. Dr. Fair corrected his testimony in response to Patent Owner's deposition questions (Ex. 2009, 16:7–22:18), and, according to Patent Owner, "Dr. Bottoms agrees with Dr. Fair's deposition testimony." PO Resp. 65 (citing Ex. 2008 ¶ 152). The experts agree that, in Tanaka II Figure 17, the dielectric constant was the same (5.4) or assumed to be the same for all reported thicknesses of HCD-SiN. Ex. 2008 ¶ 152; Ex. 2009, 17:16–18:7. The experts' agreement on this point does not undermine Dr. Fair's opinion that a POSA "would have had a reasonable expectation of success at keeping the dielectric constant below 5.5 when employing a multilayer silicon nitride etch stop." Ex. 1017 ¶ 34.

Next, Patent Owner argues that applying thin layers of Tanaka I's HCD-SiN may allow hydrogen and chlorine impurities to diffuse out of the HCD-SiN, resulting in an increased dielectric constant. PO Resp. 66. As it pertains to hydrogen impurities, that argument is not persuasive in view of the inconsistent positions taken by Patent Owner and Dr. Bottoms regarding the effects of hydrogen impurities on the dielectric constant of SiN films.

On the one hand, Patent Owner and Dr. Bottoms assert that diffusion of hydrogen and chlorine out of Tanaka I's HCD-SiN material would increase the dielectric constant of the material because hydrogen and chlorine "impurities are likely a reason for the *decreased* dielectric constant" of Tanaka I's HCD-SiN material. *Id.* (emphasis added); Ex. 2008 ¶ 163 (same). On the other hand, Patent Owner and Dr. Bottoms assert that, "[r]educing hydrogen can have the effect of lowering the dielectric constant of silicon

nitride because hydrogen impurities in silicon nitride can *increase* the dielectric constant of the material." *Id.* at 14 (emphasis added); Ex. 2008 ¶ 60 (same). We thus agree with Petitioner that Patent Owner "contradicts itself." Pet. Reply 25.

We also agree with Petitioner that Patent Owner's argument, as it pertains to chlorine impurities, is contradicted by Tanaka I, which discloses that "Cl was not detected over the detection limit up to 1000 C, and is concluded to be thermally stable." Ex. 1006, 1-2; Pet. Reply 25–26 (citing Ex. 1017 ¶ 34). There is no persuasive rebuttal to the cited testimony of Dr. Fair that a POSA "would have understood that chlorine would not diffuse out as alleged by Dr. Bottoms." Ex. 1017 ¶ 34. Moreover, aside from the unsubstantiated and speculative opinion of Dr. Bottoms (Ex. 2008 ¶ 163), Patent Owner does not direct us to persuasive evidence that hydrogen or chlorine impurities would diffuse out of silicon nitride when applied as thin layers.

Next, Patent Owner argues that "it would be understood that depositing multiple layers would increase the density of the film" and "[b]y increasing the density, the dielectric constant of the resulting film might be increased." PO Resp. 66 (citing Ex. 2008 ¶ 163). Patent Owner's argument is persuasively rebutted by Dr. Fair's testimony that a multilayer film can have a lower dielectric constant than a single layer film of the same overall thickness. Ex. 1017 ¶ 35; *see* Pet. Reply 26 (relying on Dr. Fair's testimony). As noted by Petitioner, Patent Owner's argument is inconsistent with Patent Owner's assertion in the '330 patent that multilayer deposition is one way to reduce the dielectric constant of a silicon nitride etch stop layer. Pet. Sur-

Sur-Reply 4; Ex. 1001, 5:63–6:7.

Patent Owner's argument is also contradicted by Dr. Bottoms' testimony regarding a POSA's understanding of the '330 patent's teachings about multilayer depositions. The '330 patent teaches that "multi-layer depositions . . . eliminates pinholes and produces a *denser film*." Ex. 1001, 6:3–4 (emphasis added). Dr. Bottoms testifies that, as understood by a POSA, "this means that the material overall may be *less dense* because it includes voids or chemical impurities." Ex. 2008 ¶ 40 (emphasis added). In other words, Dr. Bottoms testifies that a POSA would understand the '330 patent to teach that multilayer deposition produces a film that is less dense overall than single layer deposition. Patent Owner's argument that depositing multiple layers would increase the density of the film (PO Resp. 66) is thus contradicted by Dr. Bottoms' testimony about how a POSA would understand the teachings of the '330 patent (Ex. 2008 ¶ 40).

Patent Owner's argument is also contradicted by the teachings of Yota, and Dr. Bottoms' interpretation of those teachings. Yota discloses that a multilayer PECVD deposition process produced a lower density silicon nitride film than a single layer HDP CVD deposition process. Ex. 1023, 1-1, 1-2, 2-2, 3-2 (showing a multilayer PECVD process produced a less dense film than the HDP CVD process); *see also* Ex. 2015 ¶ 16 (Yota's HDP CVP silicon nitride process "would be understood to form a single layer of material"); *id.* ¶ 17 ("Yota reports a lower dielectric constant for the multi- layered PECVD film.").

Accordingly, after considering the parties' arguments and evidence and the record as a whole,

we are persuaded Petitioner has established by a preponderance of the evidence that claims 2 and 7 of the ’330 patent are unpatentable as obvious in view of Watatani and Tanaka I.

3. Claims 5 and 10

Claim 5 depends from claim 1 and recites “wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof.” Claim 10 depends from claim 6 and recites “wherein the first and second conductor cores contain materials selected from a group consisting of copper, gold, silver, a compound thereof, and a combination thereof.”

Petitioner directs us to substantial evidence that Watatani discloses the limitations of claims 5 and 10 by disclosing conductor cores comprising copper. Pet. 41–42, 56 (citing Ex.1005, 2:1–5, 2:42–47). Patent Owner does not contest that evidence and submits no arguments regarding claims 5 and 10 separately from its arguments regarding claims 1 and 6. We determine that Petitioner has demonstrated by a preponderance of the evidence that the limitations of claims 5 and 10 are disclosed by Watatani.

Accordingly, after considering the parties’ arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claims 5 and 10 of the ’330 patent are unpatentable as obvious in view of Watatani and Tanaka I.

III. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 1, 2, 5–7, and 10 of the ’330 patent are unpatentable.

IV. ORDER

Accordingly, in consideration of the foregoing, it is hereby: ORDERED that, based on a preponderance of the evidence, claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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APPENDIX D

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,
v.
LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01566
Patent 6,388,330 B1

Before JENNIFER MEYER CHAGNON, JOHN F. HORVATH, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.
ROESEL, *Administrative Patent Judge*.

DECISION
Denying Patent Owner's Request for Rehearing
37 C.F.R. § 42.71

I. INTRODUCTION

Patent Owner, Lone Star Silicon Innovations, LLC, timely filed a request for rehearing (Paper 10, "Request" or "Req.") of our decision instituting *inter partes* review (Paper 8, "Decision" or "Dec.") of U.S. Patent No. 6,388,330 B1 (Ex. 1001, "the '330 patent") based on a single ground asserted in the Petition (Paper 1, "Pet."): whether claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Watatani[1] in view of Tanaka I.[2] The Request seeks rehearing of our Decision as to claims 2 and 7. For the reasons given below, we deny the Request.

II. LEGAL STANDARDS

"The burden of showing a decision should be modified lies with the party challenging the decision," and the challenging party "must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed" in a paper of record. 37 C.F.R. § 42.71(d). Because Patent Owner seeks rehearing of our Decision on the Petition seeking *inter partes* review, it must show an abuse of discretion. *See* 37 C.F.R. § 42.71(c) ("When rehearing a decision on petition, a panel will review the decision for an abuse of discretion."). An abuse of discretion occurs when a "decision was based on an erroneous conclusion of law or clearly erroneous factual findings, or . . . a clear error of judgment."

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[1] Watatani, US 6,153,511, filed June 25, 1999 and issued November 28, 2000, Ex. 1005 ("Watatani").

[2] Masayuki Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47–48, Ex. 1006 ("Tanaka I").

PPG Indus., Inc. v. Celanese Polymer Specialties Co., 840 F.2d 1565, 1567 (Fed. Cir. 1988).

III. ANALYSIS

Patent Owner argues that the Board exceeded its authority and abused its discretion by instituting *inter partes* review of claims 2 and 7 based on a new ground not asserted in the Petition. Req. 2–3, 4–10. Patent Owner additionally argues that the Decision does not provide notice of the grounds on which *inter partes* review of claims 2 and 7 is instituted. *Id.* at 10–11. We are not persuaded by either argument.

We instituted *inter partes* review of claims 2 and 7 on the same ground asserted against these claims in the Petition: obviousness in view of Watatani and Tanaka I. *Compare* Dec. 20–21, *with* Pet. 4. Both the Decision and the Petition rely on another reference for evidentiary support: SST 1987.[3] Our reliance on SST 1987, however, does not transform the instituted ground into a "new ground," as argued by Patent Owner. *See* Req. 2, 3, 4, 7, 10, 11.

The Decision relies on SST 1987 in the same way the Petition does: as evidence of the knowledge of a person of ordinary skill in the art ("POSA"). Dec. 18–19; Pet. 39–40 (addressing claim 2), 53–54 (addressing claim 7); Ex. 1003 ¶¶ 45, 106. More specifically, Petitioner and its declarant, Dr. Fair, cite SST 1987 as support for their assertion that multilayer silicon nitride layers were well known in the prior art. Pet. 39, 54; Ex. 1003 ¶¶ 45, 106. Our Decision, in turn, relies on SST 1987 and Dr. Fair's testimony as sufficient evidence to support Petitioner's contention that multilayer silicon nitride

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[3] *Continuous Process CVD System*, Solid State Technology, October 1987 (Ex. 1008).

layers were known in the art. Dec. 19 (citing Pet. 15, 20, 39, 54; Ex. 1003 ¶¶ 45, 106; Ex. 1008, 1). That evidence, together with Petitioner's cited disclosures of Watatani and Tanaka I, provides a sufficient basis on which to institute review of claims 2 and 7 on the ground asserted by Petitioner.

Although Petitioner could have expressly included SST 1987 with Watatani and Tanaka I in the list of references that denominate the instituted ground, Petitioner's decision to rely instead on SST 1987 merely as support for its contention that multilayer silicon nitride layers were known in the art is not fatal to Petitioner's challenge of claims 2 and 7. Patent Owner cites no authority for the proposition that a reference relied upon to show that a claim limitation is within the knowledge of a POSA must be expressly included in the list of references that denominate the ground. As discussed above, SST 1987 is not a "new reference," as argued by Patent Owner. Req. 7. Therefore, even though SST 1987 is necessary to establish *prima facie* obviousness, there is no abuse of discretion or prejudice to Patent Owner because the Petition and the Decision each independently put Patent Owner on notice of the reference and the way in which it is relied upon by Petitioner and the Board.

IV. CONCLUSION

After considering Patent Owner's arguments for rehearing, we determine that Patent Owner has not shown that the Decision instituting *inter partes* review of claims 2 and 7 of the '330 patent was an abuse of discretion.

V. ORDER

Accordingly, it is:

ORDERED that Patent Owner's request for rehearing is *denied*.

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APPENDIX E

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,
v.
LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01566
Patent 6,388,330 B1

Before JENNIFER MEYER CHAGNON, JOHN F. HORVATH, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.
ROESEL, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

This case concerns U.S. Patent No. 6,388,330 B1. Ex. 1001 ("the '330 patent"). Petitioner, Micron Technology, Inc., filed a Petition requesting *inter partes* review of claims 1, 2, 5–7, and 10 ("the challenged claims") of the '330 patent. Paper 1 ("Pet."). Patent Owner, Lone Star Silicon Innovations, LLC, filed a Preliminary Response. Paper 7 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). An *inter partes* review may not be instituted "unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Applying that standard, we institute an *inter partes* review of claims 1, 2, 5–7, and 10 of the '330 patent ("the challenged claims") for the reasons and on the ground set forth below.

The following findings of fact and conclusions of law are not final, but are made for the sole purpose of determining whether Petitioner meets the threshold for initiating review. Any final decision shall be based on the full trial record, including any response timely filed by Patent Owner.

I. BACKGROUND

A. Related Matters

Pursuant to 37 C.F.R § 42.8(b)(2), the parties identify the following patent infringement lawsuits involving the '330 patent:

Lone Star Silicon Innovations, LLC v. Micron Technology, Inc., No. 2:16-cv-01116 (E.D. Tex. filed Oct. 7, 2016);

Lone Star Silicon Innovations, LLC v. Nanya Technology Corp., No. 2:16-cv-01117

(E.D. Tex. filed Oct. 7, 2016);

Lone Star Silicon Innovations, LLC v. Renesas Electronics Corp., No. 2:16-cv-01438 (E.D. Tex. filed Dec. 20, 2016);

Lone Star Silicon Innovations, LLC v. Semiconductor Manufacturing International Corp., No. 2:16-cv-01276 (E.D. Tex. filed Nov. 16, 2016);

Lone Star Silicon Innovations, LLC v. Toshiba Corp., No. 2:16- cv-01170 (E.D. Tex. filed Oct. 14, 2016); and

Lone Star Silicon Innovations, LLC v. United Microelectronics Corp., No. 2:16-cv-01216 (E.D. Tex. filed Oct. 31, 2016).

Pet. 2–3; Paper 3, 2 (Patent Owner Mandatory Notices).

Patent Owner identifies other *inter partes* review proceedings involving Micron Technology as Petitioner and Lone Star Silicon Innovations, LLC as Patent Owner and states that the patents involved in the other proceedings are not related to the '330 patent. Paper 3, 1.

B. Asserted Ground of Unpatentability

The Petition asserts a single ground of unpatentability with respect to the challenged claims: whether claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Watatani[1] in view of Tanaka I.[2] Pet. 4.

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[1] Watatani, US 6,153,511, filed June 25, 1999 and issued November 28, 2000, Ex. 1005 ("Watatani"). Watatani is asserted as prior art under 35 U.S.C. § 102(e). Pet. 25 n.7.

[2] Masayuki Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47–48, Ex. 1006 ("Tanaka I"). Tanaka

Petitioner supports its challenge with a Declaration of Richard Fair, Ph.D. Ex. 1003. Patent Owner supports its Preliminary Response with a Declaration of W. R. Bottoms, Ph.D. Ex. 2001.

C. The '330 Patent (Ex. 1001)

The '330 patent, titled, "Low Dielectric Constant Etch Stop Layers in Integrated Circuit Interconnects," was issued May 14, 2002 from Application No. 09/776,012, filed February 1, 2001. Ex. 1001 at (21), (22), (45), (54).

The '330 patent relates to semiconductor technology and more specifically to etch stop layers in integrated circuits. *Id.* at 1:6–8. According to the '330 patent, semiconductor devices fabricated in and on a semiconductor substrate may be interconnected using a "damascene" technique of metallization. *Id.* at 1:11–29. A "single damascene" technique is used to form a single layer of conductive interconnects, and a "dual damascene" technique is used to form multiple layers of conductive interconnects that are separated by interlayer dielectric layers, including etch stop layers, in vertically separated planes and interconnected by vertical connections or "vias." *Id.* at 1:30–34, 2:30–51. The '330 patent discloses that closely positioned, parallel conductive channels suffer from capacitive coupling effects, which can be reduced by reducing the dielectric constant of the silicon nitride etch stop layers between the channels. *Id.* at 3:32–42, 3:49–60. More specifically, the '330 patent represents that "currently used silicon nitride

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I is asserted as prior art under 35 U.S.C. § 102(b). Pet. 27 n.8. As support for public accessibility of Tanaka I, Petitioner submits the Declaration of Peter J. Rolla, an employee of the University of California San Diego Library in La Jolla California. Ex. 1009.

. . . has a dielectric constant in excess of 7.5” (*id.* at 3:39–41) and discloses that capacitive coupling effects are reduced by using an etch stop layer having a dielectric constant below 5.5 (*id.* at 3:53–54, 3:58–59).

Figures 1 and 2 of the ’330 patent show a “prior art” structure, and Figure 3 shows the invention. Ex. 1001, 4:14–20. Figures 2 and 3 of the ’330 patent are reproduced below:

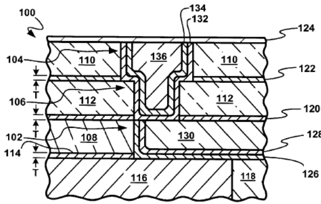

FIG. 2 (PRIOR ART)

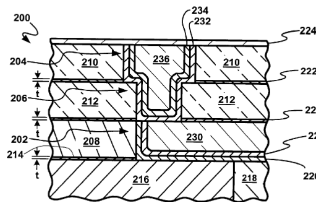

FIG. 3

Figures 2 and 3, above, show semiconductor wafers 100, 200, including dielectric layers 108, 110, 112, 208, 210, and 212; conductor cores 130, 136, 230, 236; and etch stop layers 114, 120, 122, 124, 214, 220, 222, and 224.[3] *Id.* at 4:24–32, 4:42–5:4, 5:21–53. According to the ’330 patent, Figure 3 is “similar” to Figure 2, except for the thickness of the etch stop layers, which is shown as “T” in Figure 2 and “t” in Figure 3. *Id.* at 4:18, 5:17–23, 5:66– 6:2.

Regarding the etch stop layers, the ’330 patent discloses:

> In the present invention, a half thickness, high quality, etch stop layer (compared to the prior art etch stop layer) is deposited.

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[3] Structures with 100 series reference numerals are shown in Figure 2, and structures with 200 series reference numerals are shown in Figure 3.

> For example, for silicon nitride, the dielectric constant of an etch stop layer in accordance with the present invention is about 5.5 contrasted to an excess of 7.5 in the prior art.

Id. at 5:60–65. The ’330 patent discloses processes that can be used to produce etch stop layers with a dielectric constant under 5.5, including successive deposition of multiple layers of silicon nitride, which “eliminates pinholes and produces a denser film.” *Id.* at 5:66–6:7.

D. Illustrative Claim

The ’330 patent has 10 claims, including independent claims 1 and 6. Claims 1, 2, 5–7, and 10 are challenged in the Petition. Claim 1 is reproduced below:

> 1. An integrated circuit comprising:
>
> a semiconductor substrate having a semiconductor device provided thereon;
>
> a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;
>
> a first conductor core filling the first opening and connected to the semiconductor device;
>
> an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5;
>
> a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core;
>
> a second conductor core filling the second opening and connected to the first conductor

core.

Ex. 1001, 6:54–7:2.

Claim 6 is similar to claim 1, except that it recites an additional dielectric layer (called a via dielectric layer) and an additional etch stop layer (called a channel etch stop layer), and the second conductor core fills openings in both the via and second dielectric layers. *Id.* at 7:15–8:11.

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). Under that standard, we generally give claim terms their ordinary and customary meaning, as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Petitioner does not propose any express claim constructions. Pet. 23–24. Petitioner asserts that the parties' claim construction disputes in the related district court litigation are not relevant to this proceeding. Pet. 24 n.6, 33, 34, 36–37, 41, 49.

Patent Owner acknowledges "[t]here does not appear to be a dispute as to the meaning" of "etch stop layer of silicon nitride" in claims 1 and 6 of the '330 patent, but proposes a construction for this term "for purposes of a complete record." Prelim. Resp. 15. Patent Owner's proposed construction is the construction proposed in the related district court litigation. *Compare id.*, *with* Ex. 1015, 11. As support for its proposed construction, Patent Owner relies on

Petitioner's contentions regarding the disclosure of Tanaka I. Prelim. Resp. 19–20.

After considering the Petition and the Preliminary Response, we determine that we do not need to resolve any claim construction disputes for purposes of this Decision. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy").

B. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Fair, testifies that a person of ordinary skill in the art ("POSA") would have had at least a Bachelor of Science degree in electrical engineering, material science, physics, chemistry, or a closely related field and at least five years of industry experience in the development of semiconductor process technologies and the fabrication of semiconductor devices. Ex. 1003 ¶ 18. Dr. Fair further testifies that an individual with an advanced degree in a relevant field would require less experience in developing process technologies and in fabricating semiconductor devices. *Id.* Patent Owner's declarant, Dr. Bottoms, testifies that a POSA would have held a master's degree in physics, electrical engineering or a related field and three years or more experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. Ex. 2001 ¶ 33. Neither declarant indicates that any proffered opinion would change depending on the level of ordinary skill in the art.

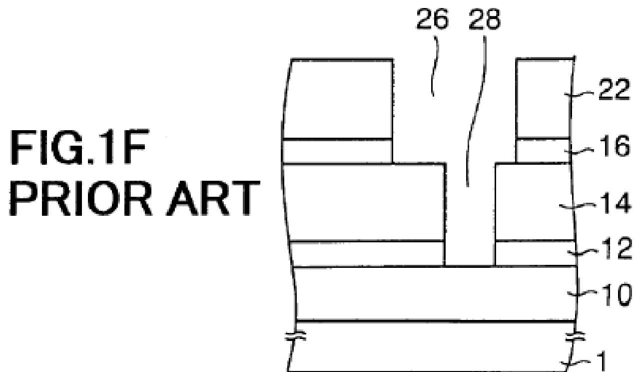
In our view, based on the record presented at this stage of the proceeding, there is little difference between the declarants' definitions of a POSA, and

the outcome of our determination whether to institute review would be the same, regardless of which definition we accept. Nevertheless, for the sake of clarity and for purposes of this Decision, we accept Dr. Bottoms' definition of a POSA. We also rely on the cited prior art references as reflecting the level of ordinary skill in the art at the time of the invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Prior Art References

1. Watatani (Ex. 1005)

Watatani discloses a semiconductor device having a multilayer interconnection structure. Ex. 1005 at (54). According to Watatani, Figures 1A–F "show a typical example of the conventional dual damascene process of forming a multilayer interconnection structure . . . ." *Id.* at 1:65–67. Petitioner relies on Watatani Figure 1F, which is reproduced below:



Watatani Figure 1F illustrates a step of a conventional dual damascene process. Ex. 1005, 1:65–67, 2:43–48, 5:32–33. The structures shown in Watatani Figure 1F include silicon (Si) substrate 1, lower interconnection pattern 10 of conductive material such as copper (Cu), etching stopper film 12 of silicon nitride (SiN), first interlayer insulation film

14 of silicon oxide (SiO_2), second etching stopper film 16 of SiN, second interlayer insulation film 22 of SiO_2, interconnection groove 26, and contact hole 28. *Id.* at 2:1–41. According to Watatani, "an insulation film (not illustrated) [is] interposed between the Si substrate 1 and the lower interconnection pattern 10." *Id.* at 2:3–5. Watatani discloses that interconnection groove 26 and contact hole 28 are filled with copper (Cu). *Id.* at 2:42–47.

According to Watatani, the multilayer interconnection structure of Figure 1F "has a drawback, due to the use of SiO_2 having a large dielectric constant, for the interlayer insulation film 14 or 22, in that the interconnection patterns tend to have a large stray capacitance." *Id.* at 2:54–58. Watatani discloses that this problem is overcome by using "an organic interlayer insulation film having a characteristically small dielectric constant." *Id.* at 2:61–64. However, conventional multilayer interconnection structures using an organic interlayer insulation film suffer from another drawback, namely that resist pattern misalignments are difficult to correct. *Id.* at 3:51–4:41. To address the resist pattern correction problem, Watatani discloses a semiconductor fabrication process that includes the steps of forming a first etching stopper film on an organic interlayer insulation film and forming a second, different etching stopper film on the first etching stopper film. *Id.* at 4:48–5:25; *see also id.* at 6:4–10 (disclosing "an etching stopper structure 81, formed of a stacking of two etching stopper layers, . . . a first etching stopper film 80 of SiN . . . and a second etching stopper film 82 of SiO_2"); Fig. 5A.

2. Tanaka I (Ex. 1006)

Tanaka I addresses the problem of parasitic capacitance associated with copper (Cu) interconnects formed by a conventional damascene process that uses high-k SiN film for the etch stopper layers. Ex. 1006, 1-1.[4] To solve this problem, Tanaka I discloses a "[n]ew low-k SiN film with a permittivity of 5.4 and high immunity for Cu diffusion and oxidation. . . ."[5] *Id.* at 1-1, 1-2. The film is formed by an ultra low temperature thermal chemical vapor deposition ("CVD") process using HexaChloroDisilane (HCD, Si_2Cl_6) as a silicon source. *Id.* at 1-1. Tanaka I refers to the new film as "HCD-SiN" and discloses a deposition process and film properties for the new film. *Id.* at 1-1, 1-2, Figs. 2–8.

Figure 1 of Tanaka I is reproduced below:

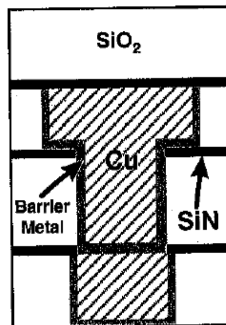


Fig.1 A schematic drawing of Cu interconnects formed by damascene process

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[4] We cite to Tanaka I and other non-patent references using the page numbers added by Petitioner followed by a hyphenated suffix ("-1" or "-2") to indicate the first or second column.

[5] Dr. Fair explains that "[t]he dielectric constant of a material, which is sometimes referred to as its permittivity and which is represented by the letter 'k,' is an intrinsic property of a material . . . ." Ex. 1003, 19 n.2.

Figure 1 of Tanaka I shows copper interconnects formed by a conventional damascene process, which requires "plural layers of high-k SiN film for a groove etch stopper and a barrier of Cu diffusion and oxidation. . . ." Ex. 1006, 1-1. As explained above, Tanaka I proposes improving upon this conventional process by using "HCD-SiN as the etch-stop and the barrier layer . . . to realize Cu damascene interconnects for high performance VLSIs." *Id.*

D. Petitioner's Asserted Ground

1. Independent Claims 1 and 6

Petitioner contends that claims 1 and 6 are unpatentable as obvious over Watatani and Tanaka I. Pet. 29–38, 42–53. Petitioner contends that a POSA would have been motivated to use the conventional or prior art dual damascene interconnect structure disclosed in Watatani, but use Tanaka I's low-k silicon nitride etch stop layers instead of conventional silicon nitride etch stop layers in order to address the issue of stray capacitance discussed in both references. *Id.* at 29, 36. Petitioner contends that Watatani Figures 1A–F and the description of those figures (Ex. 1005, 1:65–2:47) teaches or suggests all elements of claims 1 and 6, except for the dielectric constant, which Petitioner contends is taught by Tanaka I. Pet. 29–38, 42–53; *see also id.* at 35–36, 48, 51 (acknowledging that Watatani does not disclose the dielectric constant of the silicon nitride etch stop layer and citing Tanaka I, Ex. 1006, 1-1, Figs. 1, 5 for that feature). Relying on the Fair Declaration, Petitioner argues that a POSA would have been motivated to combine the teachings of Watatani and Tanaka I and would have had a reasonable expectation of success. *Id.* at 36, 48–49, 51–52, 56–60 (citing Ex. 1003 ¶¶ 95, 125, 132,

150–155; Ex. 1005, 1:23–33, 2:54–60, Figs. 1A–F; Ex. 1006, 1-1, Fig. 1; Ex. 1007,[6] 1, Fig. 1).

Patent Owner argues that Watatani and Tanaka I "address different aspects of, and provide very different solutions to, the issue of parasitic capacitance." Prelim. Resp. 44 (citing Ex. 2001 ¶ 109). Patent Owner argues that Watatani teaches away from Petitioner's proposed modification, asserting "[t]he reference is not concerned with the dielectric constant of the SiN etch stop layers, and teaches instead that the device capacitance should be controlled by using organic insulator layers," which Patent Owner characterizes as a "fundamentally different approach." *Id.* at 46–47 (citing Ex. 2001 ¶ 111). In addition, Patent Owner argues that Watatani and Tanaka I do not provide sufficient information from which a POSA could reasonably conclude that the HCD-SiN film of Tanaka I would function effectively as an etch stop in the structure and process of Watatani or that Petitioner's proposed substitution would successfully reduce the stray capacitance of Watatani's device. *Id.* at 47–53 (citing Ex. 2001 ¶¶ 113, 114, 116–122).

After considering both the Petition and Preliminary Response, we determine that Petitioner's evidence is sufficient to support its contention that it would have been obvious to substitute low dielectric constant silicon nitride etch stop layers, as disclosed in Tanaka I, for conventional silicon nitride etch stop layers in a conventional dual damascene interconnect structure, as disclosed in Figures 1A–1F of Watatani. Pet. 29, 36, 48–49, 51–

[6] Robert L. Jackson et al., *Processing and Integration of Copper Interconnects*, Solid State Technology, March 1988 ("SST 1998").

52, 56–60.

Petitioner's contention is supported by Dr. Fair's testimony that a POSA "would have been motivated to use Tanaka's low-k silicon nitride etch stop layer instead of the conventional silicon nitride etch stop layer in the dual damascene structure of Watatani in order to reduce the problem of stray capacitance discussed in both Watatani and Tanaka." Ex. 1003 ¶ 95; *see also id.* ¶¶ 40–44 (explaining that the use of low-k materials to reduce parasitic capacitance was known in the art); ¶¶ 151–155 (discussing motivation to combine and reasonable expectation of success). Petitioner's contention is further supported by Watatani, which acknowledges the problem of stray capacitance in complex, multilayer interconnection structures and discloses the substitution of interlayer insulation film having a low dielectric constant for interlayer insulation film having a large dielectric constant as a solution to the problem. Ex. 1005, 1:23–33, 2:54–64. Petitioner's contention is further supported by Tanaka I, which teaches a "low-k SiN film" for use as etch-stopper layers in an interconnect structure formed by a conventional copper damascene process. Ex. 1006, 1-1, Fig. 1.

We acknowledge Patent Owner's argument that Watatani teaches away by disclosing a different solution to the problem of stray capacitance than is claimed in the '330 patent. Prelim. Resp. 44–47. Dr. Fair addresses this issue in paragraph 155 of his testimony. Ex. 1003 ¶ 155. At this stage, we are persuaded that Petitioner's arguments and evidence are sufficient to institute review, notwithstanding Patent Owner's argument. *See Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013) ("[a] reference does not teach away . . . if it merely

expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed," quoting *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009)).

We also acknowledge Patent Owner's argument that Watatani and Tanaka I do not contain sufficient information to provide a reasonable expectation of success. Prelim. Resp. 47–53 (arguing that a POSA would need additional information regarding etch chemistries, layer thicknesses, etch selectivity versus SiO_2, and dielectric constants to determine whether Tanaka I's HCD-SiN film would function effectively as an etch stop and successfully reduce the stray capacitance of Watatani's device). At this stage, we are persuaded that Petitioner has met its burden notwithstanding Patent Owner's arguments, which can be further developed at trial.

In this regard, the relevant inquiry is whether a POSA would have had a reasonable expectation of success in modifying the prior art damascene process disclosed in Watatani's Figures 1A–1F in light of Tanaka I to achieve the claimed invention. *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016); *Slot Speaker Techs., Inc. v. Apple Inc.*, No. 2015-2038, 680 F. App'x 932, 940 (Fed. Cir. Feb. 17, 2017) (unpub.).

The integrated circuit recited in claims 1 and 6 of the '330 patent includes one or more etch stop layers having a dielectric constant below 5.5. Ex. 1001, 6:63–64, 7:24–24, 8:5–6. The challenged claims do not recite that the stray capacitance or capacitive coupling effects are reduced. Regarding stray capacitance, Tanaka I provides the same general

teaching as the '330 patent: that parasitic capacitance is reduced by replacing high dielectric constant silicon nitride etch stopper layers with low dielectric constant silicon nitride etch stopper layers. *Compare* Ex. 1006, 1-1, *with* Ex. 1001, 3:32–42, 3:49–60. Furthermore, the '330 patent does not disclose or claim any etch chemistries or etch selectivity. Although the thickness of the etch stop layer is disclosed (Ex. 1001, 6:2), the thickness of the interlayer dielectric is not disclosed, and no thicknesses are recited in the claims.

Accordingly, the parties should focus their arguments on whether a POSA would have had a reasonable expectation of successfully combining the teachings of Watatani and Tanaka I to meet the limitations of the claimed invention. *Intelligent Bio-Systems*, 821 F.3d at 1367. The applicable legal standard does not require that the prior art disclose more information than is disclosed in the '330 patent in order to provide a reasonable expectation of success. *Id.*

We have considered the testimony of Patent Owner's declarant, Dr. Bottoms. Ex. 2001 ¶¶ 109–122. To the extent that Dr. Bottoms' testimony creates a genuine issue of material fact regarding whether a POSA would have had a motivation to combine Watatani and Tanaka I and whether a POSA would have had a reasonable expectation of achieving the claimed invention, we view that dispute in the light most favorable to Petitioner at this stage of the proceeding. *See* 37 C.F.R. § 42.108(c).

After considering the arguments and evidence presented in the Petition and Preliminary Response, we are persuaded that Petitioner has demonstrated a

reasonable likelihood of prevailing on its contention that claims 1 and 6 are unpatentable as obvious over Watatani and Tanaka I.

2. Claims 2 and 7

Claim 2 depends from claim 1 and recites "wherein the etch stop layer is a multilayer structure." Ex. 1001, 7:3–4. Claim 7 depends from claim 6 and recites "wherein the via and channel etch stop layers are a multilayer structure." *Id.* at 8:12–13.

Petitioner contends that "Watatani expressly describes an etch stop layer that includes 'three or more layers' of silicon nitride." Pet. 39, 54 (citing Ex. 1005, 7:54–55). Petitioner also contends that "multilayer silicon nitride layers were well known in the prior art." *Id.* (citing Ex.1003 ¶¶ 105–107). Petitioner contends that a POSA would have been motivated to use a multilayer approach because it would improve the uniformity of the etch stop film and improve its dielectric properties by avoiding pinholes. Pet. 40–41, 55 (citing Ex. 1003 ¶¶ 107–109, 143; Ex. 1010,[7] 11:8–18); *see also* Ex. 1003 ¶ 46 (citing Ex. 1008,[8] 2-1).

Patent Owner argues that Watatani does not disclose or suggest an etch stop layer that includes three or more layers of silicon nitride, as asserted by Petitioner. Prelim. Resp. 55, 57. In addition, Patent Owner argues that Watatani's multilayer etch stop has no applicability to Watatani's Figures 1A–F embodiment and that Dr. Fair has improperly mixed features of two distinct embodiments. *Id.* at 56.

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[7] Wang et al., US 6,017,791, issued January 25, 2000 ("Wang").

[8] *Continuous Process CVD System*, Solid State Technology, October 1987 ("SST 1987").

Patent Owner argues that Wang does not provide a motivation to combine because its silicon nitride layers are not disclosed as etch stop layers. *Id.* at 58. In addition, Patent Owner argues that a POSA would have had no reasonable expectation that a multilayer etch stop would decrease the dielectric constant of Watatani's first prior art embodiment, have a dielectric constant below 5.5, or reduce the stray capacitance of parallel interconnects. *Id.* at 57–58, 59, 61.

We begin by noting that Petitioner has waived any argument that claims 2 and 7 do not require an etch stop layer that "consists of two or more layers of silicon nitride." Pet. 41 (asserting that this potential claim construction dispute in the related district court litigation "is not relevant to this Petition").

On this record, we agree with Patent Owner that Watatani does not describe an etch stop layer that includes three or more layers of silicon nitride. Prelim. Resp. 55. Petitioner cites the following disclosure in Watatani: "the etching stopper structure 81 may include three or more layers of SiO_2, SiN or SiC." Ex. 1005, 7:54–55; *see* Pet. 39. Neither Petitioner nor Dr. Fair addresses Watatani's teaching that etching stopper structure 81 includes first etching stopper film 80 and second etching stopper film 82, which have different compositions. *Id.* at (57), 4:62–65, 6:4–11, 6:18–27. Nor do Petitioner and Dr. Fair address Watatani Figure 5B, which shows that second etching stopper film 82 is selectively etched relative to first etching stopper film 80. *Id.* at 6:31–40, Fig. 5B; *see also id.* at 4:66–67 (fabrication process includes the step of "forming a first opening in said second etching stopper film so as to expose said first etching stopper film"); *see also* Ex.

2001 ¶ 92. In view of the foregoing, we are persuaded, at least at this stage of the proceeding, that Watatani does not disclose the limitations of claims 2 and 7 under a claim construction that Petitioner concedes is applicable in this proceeding. Pet. 41.

Petitioner's contentions regarding claims 2 and 7 are not, however, based solely on Watatani's disclosure of multilayer etch stops. Petitioner also contends that "multilayer silicon nitride layers were well known in the prior art." Pet. 39, 54 (citing Ex.1003 ¶¶ 105–107). According to Petitioner and Dr. Fair, multilayer silicon nitride films were produced by sequential deposition in the normal operation of the Novellus Concept One CVD tool, which was widely used in the semiconductor industry before the filing date of the '330 patent. Pet. 15, 20, 39, 54; Ex. 1003 ¶¶ 45, 106 (citing Ex. 1008, 1). Dr. Fair testifies that a POSA "knew that forming silicon nitride layers in this multi-layer fashion was advantageous, including because this approach (as embodied in the Concept One, for example) produced more uniform thin films." Ex. 1003 ¶ 46 (citing Ex. 1008, 2-1); *see also* Pet. 16 (same).

Patent Owner does not dispute Petitioner's contentions regarding multilayer silicon nitride films produced by the Novellus Concept One CVD tool. Instead, Patent Owner argues that SST 1987 (Ex. 1008) does not disclose forming HD-SiN films of the type disclosed in Tanaka I and that a POSA would have understood that depositing multiple layers would increase the density and consequently the dielectric constant of the film. Prelim. Resp. 60–61 (citing Ex. 1001, 6:3–7; Ex. 1006, 1; Ex. 2001 ¶¶ 134, 135).

After considering both the Petition and Preliminary Response, we determine that Petitioner's evidence is sufficient to support its contention that multilayer silicon nitride layers were known in the art. Pet. 15, 20, 39, 54; Ex. 1003 ¶¶ 45, 106; Ex. 1008, 1. We also determine that Petitioner's evidence is sufficient to support its contention that a POSA would have known of the advantages of a multilayer approach and would have been motivated to use that approach in view of its advantages. Pet. 16, 20, 40–41, 55; Ex. 1003 ¶¶ 46, 107–109, 143; Ex. 1008, 2-1; Ex. 1010, 11:8–18. We have considered Patent Owner's arguments, but are persuaded that Petitioner's evidence is sufficient notwithstanding those arguments.

Accordingly, after considering the arguments and evidence presented in the Petition and Preliminary Response, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its contention that claims 2 and 7 are unpatentable as obvious over Watatani and Tanaka I.

3. Claims 5 and 10

Claim 5 depends from claim 1 and recites "wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof." Claim 10 depends from claim 6 and recites "wherein the first and second conductor cores contain materials selected from a group consisting of copper, gold, silver, a compound thereof, and a combination thereof."

Petitioner contends that Watatani discloses the limitations of claims 5 and 10 by disclosing conductor cores comprising copper. Pet. 41–42, 56 (citing

Ex.1005, 2:1–5, 2:42–47).

Patent Owner submits no arguments regarding claims 5 and 10 separate from its arguments regarding claims 1 and 6.

Accordingly, after considering the arguments and evidence presented in the Petition and Preliminary Response, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its contention that claims 5 and 10 are unpatentable as obvious over Watatani and Tanaka I.

III. CONCLUSION

For the reasons stated above, we institute an *inter partes* review as set forth in the Order. At this stage of the proceeding, the Board has not made a final determination with respect to the patentability of any challenged claim or any underlying factual or legal issues.

IV. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '330 patent is instituted on the following ground of unpatentability asserted in the Petition: claims 1, 2, 5–7, and 10 as obvious under 35 U.S.C. § 103(a) in view of Watatani and Tanaka I;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '330 patent is hereby instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial; and

FURTHER ORDERED that the *inter partes* review is limited to the ground identified above, and no other ground of unpatentability is authorized.

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APPENDIX F

28 U.S.C. § 141 - Special sessions; places; notice

(a)

(1) Special sessions of the district court may be held at such places in the district as the nature of the business may require, and upon such notice as the court orders.

(2) Any business may be transacted at a special session which might be transacted at a regular session.

(b)

(1) Special sessions of the district court may be held at such places within the United States outside the district as the nature of the business may require and upon such notice as the court orders, upon a finding by either the chief judge of the district court (or, if the chief judge is unavailable, the most senior available active judge of the district court) or the judicial council of the circuit that, because of emergency conditions, no location within the district is reasonably available where such special sessions could be held.

(2) Pursuant to this subsection, any business which may be transacted at a regular session of a district court may be transacted at a special session conducted outside the district, except that a criminal trial may not be conducted at a special session outside the State in which the crime has been committed unless the defendant consents to such a criminal trial.

(3) Notwithstanding any other provision of law, in any case in which special sessions are

conducted pursuant to this section, the district court may summon jurors—

(A) in civil proceedings, from any part of the district in which the court ordinarily conducts business or the district in which it is holding a special session; and

(B) in criminal trials, from any part of the district in which the crime has been committed and, if the defendant so consents, from any district in which the court is conducting business pursuant to this section.

(4) If a district court issues an order exercising its authority under paragraph (1), the court—

(A) through the Administrative Office of the United States Courts, shall—

(i) send notice of such order, including the reasons for the issuance of such order, to the Committee on the Judiciary of the Senate and the Committee on the Judiciary of the House of Representatives; and

(ii) not later than 180 days after the expiration of such court order submit a brief report to the Committee on the Judiciary of the Senate and the Committee on the Judiciary of the House of Representatives describing the impact of such order, including—

(I) the reasons for the issuance of such order;

(II) the duration of such order;

(III) the impact of such order on litigants; and

(IV) the costs to the judiciary resulting from such order; and

(B) shall provide reasonable notice to the United States Marshals Service before the commencement of any special session held pursuant to such order.

(5) If a district court issues an order exercising its authority under paragraph (1), the court shall direct the United States marshal of the district where the court is meeting to furnish transportation and subsistence to the same extent as that provided in sections 4282 and 4285 of title 18.

35 U.S.C. § 303 - Determination of issue by Director

(a) Within three months following the filing of a request for reexamination under the provisions of section 302, the Director will determine whether a substantial new question of patentability affecting any claim of the patent concerned is raised by the request, with or without consideration of other patents or printed publications. On his own initiative, and any time, the Director may determine whether a substantial new question of patentability is raised by patents and publications discovered by him or cited under the provisions of section 301 or 302. The existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office or considered by the Office.

(b) A record of the Director's determination under subsection (a) of this section will be placed in the official file of the patent, and a copy promptly will

be given or mailed to the owner of record of the patent and to the person requesting reexamination, if any.

(c) A determination by the Director pursuant to subsection (a) of this section that no substantial new question of patentability has been raised will be final and nonappealable. Upon such a determination, the Director may refund a portion of the reexamination fee required under section 302.

35 U.S.C. § 311 - Inter partes review

(a) IN GENERAL.—

Subject to the provisions of this chapter, a person who is not the owner of a patent may file with the Office a petition to institute an inter partes review of the patent. The Director shall establish, by regulation, fees to be paid by the person requesting the review, in such amounts as the Director determines to be reasonable, considering the aggregate costs of the review.

(b) SCOPE.—

A petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.

(c) FILING DEADLINE.—A petition for inter partes review shall be filed after the later of either—

(1) the date that is 9 months after the grant of a patent; or

(2) if a post-grant review is instituted under chapter 32, the date of the termination of such post-grant review.

35 U.S.C. § 312 - Petitions

(a) REQUIREMENTS OF PETITION.—A petition filed under section 311 may be considered only if—

(1) the petition is accompanied by payment of the fee established by the Director under section 311;

(2) the petition identifies all real parties in interest;

(3) the petition identifies, in writing and with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim, including—

(A) copies of patents and printed publications that the petitioner relies upon in support of the petition; and

(B) affidavits or declarations of supporting evidence and opinions, if the petitioner relies on expert opinions;

(4) the petition provides such other information as the Director may require by regulation; and

(5) the petitioner provides copies of any of the documents required under paragraphs (2), (3), and (4) to the patent owner or, if applicable, the designated representative of the patent owner.

(b) PUBLIC AVAILABILITY.—

As soon as practicable after the receipt of a petition under section 311, the Director shall make the petition available to the public.

35 U.S.C. § 313 - Preliminary response to petition

If an inter partes review petition is filed under section 311, the patent owner shall have the right to file a preliminary response to the petition,

within a time period set by the Director, that sets forth reasons why no inter partes review should be instituted based upon the failure of the petition to meet any requirement of this chapter.

35 U.S.C. § 314 - Institution of inter partes review

(a) THRESHOLD.—

The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

(b) TIMING.—The Director shall determine whether to institute an inter partes review under this chapter pursuant to a petition filed under section 311 within 3 months after—

(1) receiving a preliminary response to the petition under section 313; or

(2) if no such preliminary response is filed, the last date on which such response may be filed.

(c) NOTICE.—

The Director shall notify the petitioner and patent owner, in writing, of the Director's determination under subsection (a), and shall make such notice available to the public as soon as is practicable. Such notice shall include the date on which the review shall commence.

(d) NO APPEAL.—

The determination by the Director whether to institute an inter partes review under this section shall be final and nonappealable.

35 U.S.C. § 315 - Relation to other proceedings or actions

(a) INFRINGER'S CIVIL ACTION.—

(1) INTER PARTES REVIEW BARRED BY CIVIL ACTION.—

An inter partes review may not be instituted if, before the date on which the petition for such a review is filed, the petitioner or real party in interest filed a civil action challenging the validity of a claim of the patent.

(2) STAY OF CIVIL ACTION.—If the petitioner or real party in interest files a civil action challenging the validity of a claim of the patent on or after the date on which the petitioner files a petition for inter partes review of the patent, that civil action shall be automatically stayed until either—

(A) the patent owner moves the court to lift the stay;

(B) the patent owner files a civil action or counterclaim alleging that the petitioner or real party in interest has infringed the patent; or

(C) the petitioner or real party in interest moves the court to dismiss the civil action.

(3) TREATMENT OF COUNTERCLAIM.—

A counterclaim challenging the validity of a claim of a patent does not constitute a civil action challenging the validity of a claim of a patent for purposes of this subsection.

(b) PATENT OWNER'S ACTION.—

An inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is

served with a complaint alleging infringement of the patent. The time limitation set forth in the preceding sentence shall not apply to a request for joinder under subsection (c).

(c) JOINDER.—

If the Director institutes an inter partes review, the Director, in his or her discretion, may join as a party to that inter partes review any person who properly files a petition under section 311 that the Director, after receiving a preliminary response under section 313 or the expiration of the time for filing such a response, determines warrants the institution of an inter partes review under section 314.

(d) MULTIPLE PROCEEDINGS.—

Notwithstanding sections 135(a), 251, and 252, and chapter 30, during the pendency of an inter partes review, if another proceeding or matter involving the patent is before the Office, the Director may determine the manner in which the inter partes review or other proceeding or matter may proceed, including providing for stay, transfer, consolidation, or termination of any such matter or proceeding.

(e) ESTOPPEL.—

(1) PROCEEDINGS BEFORE THE OFFICE.—

The petitioner in an inter partes review of a claim in a patent under this chapter that results in a final written decision under section 318(a), or the real party in interest or privy of the petitioner, may not request or maintain a proceeding before the Office with respect to that claim on any ground that the petitioner raised or reasonably could have raised during that inter partes review.

(2) CIVIL ACTIONS AND OTHER PROCEEDINGS.—
The petitioner in an inter partes review of a claim in a patent under this chapter that results in a final written decision under section 318(a), or the real party in interest or privy of the petitioner, may not assert either in a civil action arising in whole or in part under section 1338 of title 28 or in a proceeding before the International Trade Commission under section 337 of the Tariff Act of 1930 that the claim is invalid on any ground that the petitioner raised or reasonably could have raised during that inter partes review.

35 U.S.C. § 316 - Conduct of inter partes review

(a) REGULATIONS.—The Director shall prescribe regulations—

(1) providing that the file of any proceeding under this chapter shall be made available to the public, except that any petition or document filed with the intent that it be sealed shall, if accompanied by a motion to seal, be treated as sealed pending the outcome of the ruling on the motion;

(2) setting forth the standards for the showing of sufficient grounds to institute a review under section 314(a);

(3) establishing procedures for the submission of supplemental information after the petition is filed;

(4) establishing and governing inter partes review under this chapter and the relationship of such review to other proceedings under this title;

(5) setting forth standards and procedures for discovery of relevant evidence, including that such discovery shall be limited to—

(A) the deposition of witnesses submitting affidavits or declarations; and

(B) what is otherwise necessary in the interest of justice;

(6) prescribing sanctions for abuse of discovery, abuse of process, or any other improper use of the proceeding, such as to harass or to cause unnecessary delay or an unnecessary increase in the cost of the proceeding;

(7) providing for protective orders governing the exchange and submission of confidential information;

(8) providing for the filing by the patent owner of a response to the petition under section 313 after an inter partes review has been instituted, and requiring that the patent owner file with such response, through affidavits or declarations, any additional factual evidence and expert opinions on which the patent owner relies in support of the response;

(9) setting forth standards and procedures for allowing the patent owner to move to amend the patent under subsection (d) to cancel a challenged claim or propose a reasonable number of substitute claims, and ensuring that any information submitted by the patent owner in support of any amendment entered under subsection (d) is made available to the public as part of the prosecution history of the patent;

(10) providing either party with the right to an oral hearing as part of the proceeding;

(11) requiring that the final determination in an inter partes review be issued not later than 1 year after the date on which the Director notices the institution of a review under this chapter, except that the Director may, for good cause shown, extend the 1-year period by not more than 6 months, and may adjust the time periods in this paragraph in the case of joinder under section 315(c);

(12) setting a time period for requesting joinder under section 315(c); and

(13) providing the petitioner with at least 1 opportunity to file written comments within a time period established by the Director.

(b) CONSIDERATIONS.—

In prescribing regulations under this section, the Director shall consider the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under this chapter.

(c) PATENT TRIAL AND APPEAL BOARD.—

The Patent Trial and Appeal Board shall, in accordance with section 6, conduct each inter partes review instituted under this chapter.

(d) AMENDMENT OF THE PATENT.—

(1) IN GENERAL.—During an inter partes review instituted under this chapter, the patent owner may file 1 motion to amend the patent in 1 or more of the following ways:

(A) Cancel any challenged patent claim.

(B) For each challenged claim, propose a reasonable number of substitute claims.

(2) ADDITIONAL MOTIONS.—

Additional motions to amend may be permitted upon the joint request of the petitioner and the patent owner to materially advance the settlement of a proceeding under section 317, or as permitted by regulations prescribed by the Director.

(3) SCOPE OF CLAIMS.—

An amendment under this subsection may not enlarge the scope of the claims of the patent or introduce new matter.

(e) EVIDENTIARY STANDARDS.—

In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.

35 U.S.C. § 317 - Settlement

(a) IN GENERAL.—

An inter partes review instituted under this chapter shall be terminated with respect to any petitioner upon the joint request of the petitioner and the patent owner, unless the Office has decided the merits of the proceeding before the request for termination is filed. If the inter partes review is terminated with respect to a petitioner under this section, no estoppel under section 315(e) shall attach to the petitioner, or to the real party in interest or privy of the petitioner, on the basis of that petitioner's institution of that inter partes review. If no petitioner remains in the inter partes review, the Office may terminate the review or proceed to a final written decision under section 318(a).

(b) AGREEMENTS IN WRITING.—

Any agreement or understanding between the patent owner and a petitioner, including any collateral agreements referred to in such agreement or understanding, made in connection with, or in contemplation of, the termination of an inter partes review under this section shall be in writing and a true copy of such agreement or understanding shall be filed in the Office before the termination of the inter partes review as between the parties. At the request of a party to the proceeding, the agreement or understanding shall be treated as business confidential information, shall be kept separate from the file of the involved patents, and shall be made available only to Federal Government agencies on written request, or to any person on a showing of good cause.

35 U.S.C. § 318 - Decision of the Board

(a) FINAL WRITTEN DECISION.—

If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d).

(b) CERTIFICATE.—

If the Patent Trial and Appeal Board issues a final written decision under subsection (a) and the time for appeal has expired or any appeal has terminated, the Director shall issue and publish a certificate canceling any claim of the patent finally determined to be unpatentable, confirming any claim of the patent determined to be patentable, and incorporating in the patent by operation of the

certificate any new or amended claim determined to be patentable.

(c) INTERVENING RIGHTS.—

Any proposed amended or new claim determined to be patentable and incorporated into a patent following an inter partes review under this chapter shall have the same effect as that specified in section 252 for reissued patents on the right of any person who made, purchased, or used within the United States, or imported into the United States, anything patented by such proposed amended or new claim, or who made substantial preparation therefor, before the issuance of a certificate under subsection (b).

(d) DATA ON LENGTH OF REVIEW.—

The Office shall make available to the public data describing the length of time between the institution of, and the issuance of a final written decision under subsection (a) for, each inter partes review.

35 U.S.C. § 319 - Appeal

A party dissatisfied with the final written decision of the Patent Trial and Appeal Board under section 318(a) may appeal the decision pursuant to sections 141 through 144. Any party to the inter partes review shall have the right to be a party to the appeal.