APPENDIX

APPENDIX A

NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

IYM TECHNOLOGIES LLC,
Appellant

v.

RPX CORPORATION, ADVANCED MICRO DEVICES, INC.,
Appellees

2019-1761

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01886.

JUDGMENT

MICHAEL DEVINCENZO, King & Wood Mallesons LLP, New York, NY, argued for appellant. Also represented by ROBERT WHITMAN, ANDREA PACELLI, CHARLES WIZENFELD.

NATHAN R. SPEED, Wolf, Greenfield & Sacks, PC, Boston, MA, argued for appellees. Also represented by RICHARD GIUNTA, BRYAN S. CONLEY, RANDY J. PRITZKER, ANANT KUMAR SARASWAT.

THIS CAUSE having been heard and considered, it is ORDERED and ADJUDGED:

PER CURIAM (LOURIE, MOORE, and HUGHES, *Circuit Judges*).

AFFIRMED. See Fed. Cir. R. 36.

ENTERED BY ORDER OF THE COURT

March 9, 2020
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

APPENDIX B

NOTE: This order is nonprecedential.

United States Court of Appeals for the Federal Circuit

IYM TECHNOLOGIES LLC,
Appellant

v.

RPX CORPORATION, ADVANCED MICRO DEVICES, INC.,
Appellees

2019-1762

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01888.

Before LOURIE, MOORE, and HUGHES, *Circuit Judges*.

PER CURIAM.

O R D E R

RPX Corporation petitioned for inter partes review of claims of 1–11, 13, and 14 of U.S. Patent 7,448,012, owned by IYM Technologies LLC. After that review, the Patent Trial and Appeal Board ("the Board") held that claims 1–9, 11, 13, and 14 of the '012 patent are unpatentable. See *RPX Corp. v. IYM Techs. LLC*, No. IPR2017-01888 (PTAB March 6, 2019). IYM appeals.

In a separate appeal, we recently affirmed a decision by the Board holding claims 1–14 of the same '012 patent unpatentable. *IYM Techs. LLC v. RPX Corp.*, No. 19-1761 (Fed. Cir. March 9, 2020).

IT IS ORDERED THAT:

Accordingly, this appeal is dismissed as moot in light of our affirmance in *IYM Techs. LLC v. RPX Corp.*, No. 19-1761 (Fed. Cir. March 9, 2020), which invalidated all of the claims at issue in this appeal.

FOR THE COURT

March 13, 2020 — /s/ Peter R. Marksteiner
Date — Peter R. Marksteiner
Clerk of Court

APPENDIX C

Trials@uspto.gov Paper No. 35
571.272.7822 Filed: March 6, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RPX CORPORATION and ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

IYM TECHNOLOGIES LLC,
Patent Owner.

Case IPR2017-01886
Patent 7,448,012 B1

Before MICHAEL R. ZECHER, MINN CHUNG, and CARL L. SILVERMAN, *Administrative Patent Judges*.

ZECHER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Petitioner, RPX Corporation and Advanced Micro Devices, Inc. (collectively, "RPX"), filed a Petition requesting an *inter partes* review of claims 1–14 of U.S. Patent No. 7,448,012 B1 (Ex. 1001, "the '012 patent"). Paper 1 ("Pet."). Patent Owner, IYM Technologies LLC ("IYM"), filed a Preliminary Response. Paper 8. Taking into account the arguments presented in IYM's Preliminary Response, we determined that the information presented in the Petition established that there was a reasonable likelihood that RPX would prevail in challenging at least one of claims 1–14 of the '012 patent as unpatentable under 35 U.S.C. § 103(a). Pursuant to 35 U.S.C. § 314, we instituted this *inter partes* review on March 8, 2018, as to all of the challenged claims and all grounds raised in the Petition. Paper 9 ("Dec. on Inst.").

During the course of trial, IYM filed a Patent Owner Response (Paper 14, "PO Resp."), RPX filed a Reply to the Patent Owner Response (Paper 20, "Pet. Reply"), and, with our authorization, IYM filed a Sur-Reply to the Reply (Paper 24, "PO Sur-Reply"). Each party was afforded the opportunity to file a one-page paper that identifies purported improper/proper arguments raised in the Sur-Reply. Papers 27, 30. A consolidated oral hearing with related Case IPR2017-01888 was held on December 11, 2018, and a transcript of the hearing is included in the record. Paper 34 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–14 of the '012 patent. For the reasons discussed below, we hold that RPX has demonstrated by a preponderance of the evidence that these claims are unpatentable under § 103(a).

A. Related Matters

The parties indicate that the ’012 patent is involved in a district court case captioned *IYM Technologies LLC v. Advanced Micro Devices, Inc.*, No. 1:16-cv-00649-GMS (D. Del.). Pet. viii; Paper 4, 1. In addition to this Petition, RPX filed another petition challenging the patentability of claims 1–11, 13, and 14 of the ’012 patent (Case IPR2017-01888). Pet. viii; Paper 4, 1. A Final Written Decision for Case IPR2017-01888 is being entered concurrently.

B. The ’012 Patent

The ’012 patent, titled “Methods and System for Improving Integrated Circuit Layout,” issued November 4, 2008, from U.S. Patent Application No. 10/907,814, filed on April 15, 2005. Ex. 1001, [54], [45], [21], [22]. The ’012 patent claims priority to the following two provisional applications: (1) U.S. Provisional Application No. 60/603,758, filed on August 23, 2004; and (2) U.S. Provisional Application No. 60/564,082, filed on April 21, 2004. *Id.* at [60].

The ’012 patent generally relates to integrated circuit (“IC”) manufacturing and, in particular, to a method and system for generating and optimizing the layout artwork of an IC. Ex. 1001, 1:11–13. As background, the ’012 patent discloses that, in modern processing technology, the manufacturing yield of ICs (i.e., a measure of functioning devices in semiconductor testing) depends on their layout construction. *Id.* at 1:17–19. For a given manufacturing process, a set of design rules are applied during chip layout in order to avoid geometry patterns that cause chip failures. *Id.* at

1:19–21. These design rules guarantee the yield by limiting layout geometry parameters, such as minimum spacing, minimal line width, etc. *Id.* at 1:21–23. Conventional layout construction systems cover the worst case scenario for all chips by applying these design rules over a wide chip area and to entire classes of circuits. *Id.* at 1:24–27.

The '012 patent discloses that, in modern processing technology, many layout features may interact during chip processing. Ex. 1001, 1:29–31. These feature dependent interactions are difficult to capture with precise design rules and, as a result, sufficiently relaxed global design rules are implemented in order to guarantee the yield. *Id.* at 1:33–36. According to the '012 patent, there are two drawbacks to this approach: (1) it clearly wastes chip area; and (2) determining the worst case scenario in all chips is a non-trivial task that consumes engineering resources. *Id.* at 1:37–40. The '012 patent also discloses that some emerging processing technologies prefer one spatial direction over the other. *Id.* at 1:41–42. Existing layout generation systems, however, use identical minimal spacing and minimal width rules for both directions, which, according to the '012 patent, leads to wasted chip area and underutilization of processing capabilities because the design rules must cover the worst case scenario in both directions. *Id.* at 1:42–46.

The '012 patent purportedly addresses these and other problems by providing a method and system for forming layout constraints to account for local and orientation processing dependencies. Ex. 1001, 1:51–54. By combining a local process modification value, which represents an additional safeguard beyond an original design rule constraint, with the original design rule constraint itself, it effectively creates a new constraint for every unique local situation. *Id.* at 1:55–64, 4:3–5. This mechanism adds extra safeguards to design rule formulation and improves chip yield by eliminating processing hotspots. *Id.* at 1:64–67, 4:5–6.

C. Illustrative Claim

Claim 1 is the only independent claim at issue. Independent claim 1 is directed to "[a] method for generating design layout artwork implemented in a computer." Ex. 1001, 8:16–17. Claims 2–14 directly depend from independent claim 1. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A method for generating design layout artwork implemented in a computer, comprising:
>
> receiving a design layout comprising a plurality of layout objects residing on a plurality of layers;
>
> receiving descriptions of manufacturing process;
>
> constructing a system of initial constraints among said layout objects;
>
> computing local process modifications to change said initial constraints using said descriptions of manufacturing process;
>
> constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints;
>
> enforcing said new local constraint distances; and

updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances;

whereby a new layout is produced that has increased yield and performance.

Ex. 1001, 8:15–35.

D. Prior Art Relied Upon

RPX relies upon the prior art references set forth in the table below:

Inventor[1]	U.S. Patent No.	Relevant Dates	Exhibit No.
Côté	6,745,372 B2	issued June 1, 2004, filed Apr. 5, 2002	1004
Bamji	5,663,891	issued Sept. 2, 1997, filed Apr. 3, 1996	1005
Kroyan	7,523,429 B2	issued Apr. 21, 2009, filed Feb. 18, 2005	1006
Cobb	6,249,904 B1	issued June 19, 2001, filed Apr. 30, 1999	1007

[1] For clarity and ease of reference, we only list the first named inventor.

E. Instituted Grounds of Unpatentability

We instituted a trial based on the asserted grounds of unpatentability ("grounds") set forth in the table below. Dec. on Inst. 31.

Reference(s)	Basis	Challenged Claim(s)
Côté	§ 103(a)	1–3, 5, 13, and 14
Côté and Bamji	§ 103(a)	1–3, 5, 10, 11, and 13
Côté, Bamji, and Kroyan	§ 103(a)	3, 4, and 6–9
Côté, Bamji, and Cobb	§ 103(a)	12

II. ANALYSIS

A. Claim Construction

In an *inter partes* review proceeding filed before November 13, 2018, claim terms of an unexpired patent are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2018).[2] Under the broadest reasonable interpretation standard, claim terms are generally given their ordinary and customary meaning, as would be understood by one of ordinary skill

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[2] A different rule applies for petitions filed on or after November 13, 2018. Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b)).

in the art, in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In the Decision on Institution, because there was no dispute between the parties regarding claim construction at the preliminary stage, we did not construe explicitly any claim term of the '012 patent. Dec. on Inst. 6–7 (citing *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the *extent necessary to resolve the controversy.'" (quoting Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)))). After reviewing the record developed during trial, we maintain that no claim term of the '012 patent requires an explicit construction for purposes of this Final Written Decision.

In its Patent Owner Response, IYM proposes constructions for the following claim terms: (1) "constraints"; (2) "enforcing said new local constraint distances"; (3) "description(s) of manufacturing process"; and (4) "width," "space," "overlap," "enclosure," and "extension." PO Resp. 14–22. Beginning with IYM's proposed constructions for the claim terms "constraints," "description(s) of manufacturing process", and "width," "space," "overlap," "enclosure," and "extension," there is no dispute between the parties regarding the proper constructions for these claim terms. *Compare* PO Resp. 14–17, 22, *with* Pet. 17–19, 28–29.

Turning to IYM's proposed construction for the claim term "enforcing said new local constraint distances," IYM contends that this claim term should be construed as "finding solutions (i.e., adjustments to the layout) that remove violations of the new local constraint distances." PO Resp. 17. IYM, however, asserts that it only offers an explicit construction to "crystallize the issues with respect to the Allan reference in [Case] IPR2017-01888." *Id.* at 21. Indeed, IYM does not argue separately whether RPX properly relies on Côté, which serves as the primary reference in the grounds based on obviousness raised in this proceeding, to teach or suggest the claim term "enforcing said new local constraint distances." *See generally id.* at 30–57, 62–65 (limiting its arguments to whether Côté teaches or suggests the "local process modifications" and "new local constraint distances," as recited in independent claim 1); *see also* Pet. Reply 5 ("IYM does not challenge that Côté meets the 'enforcing' limitation, and disputes only whether 'the Allan reference in [Case] IPR2017-01888' does. [PO Resp.] 17, 21; . . . Ex. 1027, 252:15–253:9 (confirming that construction of 'enforcing' limitation is not relevant to opinions regarding Côté)."). Because IYM does not challenge RPX's arguments and evidence as to whether Côté teaches or suggests the claim term "enforcing said new local constraint distances," we need not construe explicitly this claim term for purposes of this Final Written Decision. *See Nidec Motor Corp.*, 868 F.3d at 1017.

B. Obviousness Over the Teachings of Côté

RPX contends that claims 1–3, 5, 13, and 14 of the '012 patent are unpatentable under § 103(a) over the teachings of Côté. Pet. 21–40. RPX explains how Côté teaches or suggests the subject matter of each challenged claim, and provides reasoning as to the reasonable inferences one of ordinary skill in the art would be expected to draw from the teachings of that reference. *Id.* RPX also relies on the Declaration of Dr.

Nagel to support its positions. Ex. 1002 ¶¶ 138–187, 252–263. In its Patent Owner Response, IYM presents a number of arguments, most of which focus on whether Côté teaches or suggests "computing local process modifications to change said initial constraints using said descriptions of manufacturing process" and "constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints," as recited in independent claim 1. PO Resp. 30–57. IYM relies upon the Declaration of Dr. Bernstein to support its positions. Ex. 2012 ¶¶ 73–112.

We begin our analysis with the principles of law that generally apply to a ground based on obviousness, followed by an assessment of the level of skill in the art, proceeded by a brief overview of Côté, and then we address the parties' contentions with respect to the claims at issue in this asserted ground.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Level of Skill in the Art

There is evidence in the record before us that enables us to determine the knowledge level of a person of ordinary skill in the art. Relying on the testimony of its declarant, Dr. Nagel, RPX asserts that a person of ordinary skill in the art as of April 2004, which is the earliest priority date on the face of the '012 patent, would be an individual who possesses "a bachelor's degree in Electrical Engineering or the equivalent, along with at least two years of experience in developing and/or researching integrated circuit technology." Pet. 16 (citing Ex. 1002 ¶¶ 30–32). IYM's declarant, Dr. Bernstein, generally agrees with the assessment of RPX and Dr. Nagel, but further clarifies that "a person of ordinary skill in the art would have had a sufficient familiarity with [electronic design automation] tools to be able to competently use such tools and understand their operation." PO Resp. 12–13 (citing Ex. 1002 ¶ 31; Ex. 2012 ¶¶ 26–29).

We do not discern a material difference between the assessments advanced by the declarants, nor does either party premise its arguments exclusively on its assessment of the level of skill in the art. Moreover, each party's declarant appears to meet or exceed both parties' assessments (see Ex. 1002 ¶¶ 2–13; Ex. 1003; Ex. 2012 ¶¶ 3–19, Curriculum Vitae), and either assessment of the level of skill in the art is consistent with the '012 patent and the asserted prior art. We, therefore, adopt Dr. Nagel's assessment and apply it to our obviousness evaluation below, but note that our conclusions would remain the same under Dr. Bernstein's assessment.

3. Côté Overview

Côté generally relates to the process of designing an IC and, in particular, to simulating effects of a manufacturing process on an IC to enhance process latitude and/or reduce layout size. Ex. 1004, 1:9–13. Figure 5 of Côté, reproduced below, illustrates generating and enhancing the layout of an IC in accordance with one embodiment. *Id.* at 3:53–55, 5:8–10.

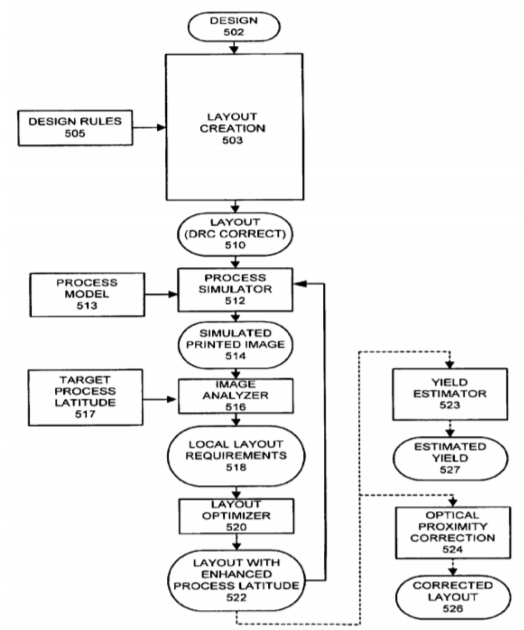


FIG. 5

Figure 5, reproduced above, depicts layout creation process 503 that receives design 502 and "ensures that the resulting layout 510 satisfies a set of design rules 505." Ex. 1004, 5:12–14. Next, layout 510 is "[fed] through process simulator 512," which, in turn, "uses a process model 513 to generate a simulated printed image 514 for the layout." *Id.* at 5:17–19. Simulated printed image 514 "may include a number of printed images generated using different process parameters." *Id.* at

5:19–22. This allows process simulator 512 to determine how the changes in process parameters will affect the printed image. *Id.* at 5:22–24.

Côté further discloses that "image analyzer 516 uses the simulated printed image 514 to generate local layout requirements 518 to optimize the process latitude and/or layout characteristics" (e.g., area). Ex. 1004, 5:29–32. These "additional constraints 518" are "[fed] into a layout optimizer 520, which further optimizes the layout." *Id.* at 5:32–35. In at least one instance, "layout optimizer 520 attempts to update the layout to produce a layout 522 with enhanced process latitude." *Id.* at 5:36–38. "[L]ayout 522 can additionally feed into yield estimator 523 to produce an estimated yield 527 for the [IC]." *Id.* at 5:55–57. According to Côté, "[this] simulation process can be applied to the enhanced layout in an iterative fashion to further improve process latitude for the layout." *Id.* at 5:58–60.

4. Claim 1

In its Petition, RPX primarily relies on the generation and enhancement of a layout as illustrated in Figure 5 of Côté and its corresponding description to teach all of the limitations of independent claim 1. Pet. 24–38. Beginning with the recitation in the preamble of "[a] method for generating design layout artwork implemented in a computer," RPX argues that Côté teaches this intended use language because it discloses techniques implemented by various software components, including an image analyzer 516 that generates local layout requirements 518 and layout optimizer 520 that optimizes the layout and generates enhanced layout 522. *Id.* at 24 (citing Ex. 1004, 2:48, 6:60–63; Ex. 1002 ¶ 137).

The first method step of independent claim 1 is "receiving a design layout comprising a plurality of layout objects residing on a plurality of layers." Ex. 1001, 8:18–19. RPX argues that Côté teaches this "receiving" method step because the embodiment illustrated in Figure 5 indicates that layout creating process 503 receives design 502. Pet. 24 (citing Ex. 1004, 2:38–44, 4:51–52, 5:13–17, Figs. 1, 6, 7; Ex. 1002 ¶ 139). Relying on the testimony of Dr. Nagel, RPX argues that one of ordinary skill in the art would have understood that Côté's layout (such as layout 510 disclosed in the context of Figure 5) includes a plurality of layout objects, which, in turn, reside on a plurality of layers. *Id.* at 25 (citing Ex. 1002 ¶ 140). RPX also directs us to Figure 7 of Côté as one example of a simulated printout image produced from a layout that includes a plurality of objects and multiple layers. *Id.* at 25–26 (citing Ex. 1004, 5:18–30, 6:31, Fig. 7; Ex. 1002 ¶¶ 141–149).

The second method step of independent claim 1 is "receiving descriptions of manufacturing process." Ex. 1001, 8:20. RPX argues that Côté teaches this "receiving" method step because layout creation process 503 illustrated in Figure 5 receives design rules 505 that "specify a number of constraints, such as minimum spacings or minimum line widths, to increase the likelihood that the finished [IC] functions properly in spite of different manufacturing effects." Pet. 27 (quoting Ex. 1004, 1:58–63) (citing Ex. 1004, 5:12–14, Fig. 5). RPX also argues that Côté teaches this "receiving" method step because simulator 512 uses process model 513 to generate simulated printed image 514 for the layout. *Id.* According to RPX, Côté's simulated printed image 514 may include a number of printed images generated using different process parameters so as to "determine how the printed image will be affected by changes in process parameters." *Id.* (quoting Ex. 1004, 5:18–24). Relying on the testimony of Dr. Nagel, RPX asserts that one of ordinary skill in the art would have understood that both Côté's design rules and simulation models serve as examples of information describing a manufacturing process. *Id.* at 26–27 (citing Ex. 1002 ¶¶ 150–154).

The third method step of independent claim 1 is "constructing a system of initial constraints among said layout objects." Ex. 1001, 8:21–22. RPX argues that IYM should be held to its proposed construction of the claim term "constraints" in the related district court case as "limits on geometry parameters of the layout objects in the design layout." Pet. 28 (citing Ex. 1017, 4–6). As support for this construction, RPX directs us to various disclosures in the specification of the '012 patent. *Id.* (citing Ex. 1001, 3:10–11, 3:16–17, 3:28–29). Applying the aforementioned construction of the claim term "constraints," RPX argues that Côté similarly discloses determining constraints for layout 510 using design rules 505. *Id.* at 29 (citing Ex. 1004, 1:59–60, 4:46–54, 5:12–14). Relying on the testimony of Dr. Nagel, RPX argues that one of ordinary skill in the art would have appreciated that Côté's process of applying design rules 505 to layout 510 is identical to the parlance of the '012 patent of "constructing a system of initial constraints among said layout objects." *Id.* (citing Ex. 1002 ¶ 158).

The fourth method step of independent claim 1 is "computing local process modifications to change said initial constraints using said descriptions of manufacturing process." Ex. 1001, 8:23–25. RPX argues that Côté teaches this "computing" method step because it discloses simulating the effects of manufacturing processes on layout 510 in order to identify problem areas from which local layout requirements may be derived. Pet. 31 (citing Ex. 1004, 2:37–46, 5:17–29; Ex. 1002 ¶¶ 162–167). According to RPX, after identifying problem areas in layout 510, Côté uses those problem areas to generate local layout requirements 518 to optimize latitude and/or layout characteristics (e.g., area). *Id.* (citing Ex. 1004, 2:8–10, 2:45–47, 5:31–36, 6:31–40). RPX asserts that Côté discloses generating layout requirements 518 from running simulations (i.e., "descriptions of manufacturing process"), and using those local layout requirements 518 to change the "initial constraints," which constitutes the claimed "local process modifications." *Id.* at 32 (citing Ex. 1004, 3:10–12, 5:18–31).

The fifth method step of independent claim 1 is "constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints." Ex. 1001, 8:26–28. RPX argues that Côté teaches this "constructing" method step because it discloses feeding additional constraints 518 generated from local process modifications into layout optimizer 520, "which further optimizes the layout." Pet. 33 (quoting Ex. 1004, 5:31–36). According to RPX, Côté's newly constructed constraint distances (i.e., additional constraints 518) are applied to local areas of the layout during the optimization process and, therefore, constitute the claimed "new local constraint distances." *Id.* (citing Ex. 1004, 2:10–12, 5:9–33, 6:9–17, 6:31–40). Relying on the testimony of Dr. Nagel, RPX asserts that Côté discloses generating the newly constructed constraint distances based on both the original design rules, as well as the local process modifications determined from running simulations. *Id.* at 33–34 (citing Ex. 1002 ¶¶ 168–171).

The sixth method step of independent claim 1 is "enforcing said new local constraint distances." Ex. 1001, 8:29. RPX argues that the '012 patent discloses enforcing constraints by executing an optimization process incorporating those constraints. Pet. 35 (citing Ex. 1001, 3:65–67, 4:17–67). RPX argues that Côté teaches this "enforcing" method step because, similar to the optimization approach disclosed in the '012 patent, Côté discloses feeding additional constraints 518 into layout optimizer 520 to produce enhanced layout 522 with improved process latitude. *Id.* (citing Ex. 1004, 5:32–33). According to RPX, Côté's production of enhanced layout 522 confirms that additional constraints 518 are enforced. *Id.* at 35–36 (citing Ex. 1004, 6:52–59; Ex. 1002 ¶¶ 176–178).

The seventh method step of independent claim 1 is "updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances." Ex. 1001, 8:30–32. RPX argues that Côté teaches this "updating" method step because layout optimizer 520 produces enhanced layout 522, which also may be used to improve process yield by feeding it into yield estimator 523 to produce estimated yield 527. Pet. 36 (citing Ex. 1004, 2:48–64, 5:8–50). RPX also directs us to Figure 6 of Côté as one example of updating the coordinates of layout shapes based on an enhanced layout. *Id.* (citing Ex. 1004, 6:7–12, Fig. 6). RPX asserts that Côté's optimization results are the claimed "solutions obtained from enforcing said new local constraint distances," and that Côté's movement of the objects in the enhanced layout amounts to the claimed "updating the coordinate variables of layout objects" according to the solutions produced by layout optimizer 520 in enforcing local layout requirements 518. *Id.*

The last limitation of independent claim 1 is "whereby a new layout is produced that has increased yield and performance." Ex. 1001, 8:33–34. RPX argues that IYM should be held to its position in the related district court case that the "whereby" clause is not limiting. Pet. 37 (citing Ex. 1017, 15). RPX further argues that, to the extent we determine that the "whereby" clause is limiting, Côté discloses this limitation because it uses layout optimizer 520 to enhance layout 510 in order to improve process latitude. *Id.* (citing Ex. 1004, 5:8–35). Relying on the testimony of Dr. Nagel, RPX asserts that a person of ordinary skill in the art would have understood that (1) an improvement to process latitude would improve yield; and (2) compaction could increase the performance of an IC (e.g., by reducing worst case path delay). *Id.* at 37–38 (citing Ex. 1002 ¶ 185). RPX asserts, therefore, that Côté's IC resulting from the new enhanced layout would have increased yield and performance. *Id.*

In its Patent Owner Response, IYM's arguments can be grouped as follows: (1) RPX blurs the line between anticipation and obviousness; (2) Côté does not teach or suggest "computing local process modifications to change said initial constraints using said descriptions of manufacturing process"; (3) Côté does not teach or suggest "constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints"; and (4) the remaining arguments. We address these groupings of arguments in turn. *See* PO Resp. 30–57.

a. The Relevant Inquiry Is One of Obviousness—Not Anticipation

As an initial matter, we address IYM's vague assertions implying RPX's asserted ground based on Côté alone is actually one of anticipation—not obviousness. As one example, when addressing whether RPX may rely on the teachings of Côté together with Dr. Nagel's supporting testimony, IYM asserts that "'[a]n expert's conclusory testimony, unsupported by the documentary evidence, cannot supplant the requirement of anticipatory disclosure in the prior art reference itself.'" PO Resp. 2 (quoting *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1473 (Fed. Cir. 1997)); *see also id.* at 43 (arguing the same). As another example, when arguing that a person of ordinary skill in the art cannot provide the limitations purportedly missing from Côté, IYM states that "Côté does not anticipate the challenged claims." *Id.* at 54. Yet another example is IYM's argument that "[RPX] appear[s] to 'confuse[] anticipation . . . with obviousness, which, though anticipation is the epitome of obviousness, are separate and distinct concepts.'" *Id.* at 55 (quoting *Jones v. Hardy*, 727 F.2d 1524, 1529 (Fed. Cir. 1984)).

Similar to the arguments presented at the preliminary stage, we understand IYM to assert that the ground based on Côté alone blurs the line between anticipation and obviousness. Contrary to IYM's assertion, RPX does not argue that Côté anticipates the challenged claims, but rather it argues that the teachings of Côté together with the background knowledge of one of ordinary skill in the art renders the challenged claims obvious. Pet. 21–40; *see also* PO Resp. 54 (admitting that, "in fact [RPX] do[es] not even argue anticipation by Côté"). As support for this and other obviousness grounds raised in the Petition, RPX explains:

> The claims call out specific features that do not contribute to the purported inventiveness of the '012 patent and are instead the type of information that publications in this field typically assume is within the reader's knowledge and do not explicitly discuss. For this reason, . . . obviousness grounds are presented rather than anticipation, even where a single reference is cited. Dr. Nagel's testimony is cited for these well-known features, together with supporting evidence.

Pet. 8. Under the circumstances described by RPX, it is appropriate to apply a single prior art reference—in this case, Côté—together with the background knowledge of one of ordinary skill in the art—as evidenced by Dr. Nagel's supporting testimony—in analyzing obviousness. *See Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1346–47 (Fed. Cir. 2018) ("Though less common, in appropriate circumstances, a patent can be obvious in light of a single prior art reference if it would have been obvious to modify the reference to arrive at the [claimed] invention.") (quoting *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016)); *see also Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (affirming the Board's conclusion that claims were obvious based on one prior art reference alone notwithstanding patent owner's argument that the ground at issue would have been more properly raised under 35 U.S.C. § 102).

b. Côté Teaches "Local Process Modifications"

In its Patent Owner Response, IYM contends that it is unclear what teachings in Côté satisfy the claimed "local process modifications" and "new local constraint distances." PO Resp. 32. IYM argues that the diversity of opinions between RPX's and Dr. Nagel's strained reading of Côté and the Board's preliminary findings indicate that Côté is susceptible to fundamentally different readings, none of which renders obvious the challenged claims. *Id.* at 32–33 (citing Pet. 34–35; Ex. 2013, 183:20–184:14, 185:14–21, 186:10–24, 236:23–237:6; Dec. on Inst. 19; Ex. 2012 ¶ 76). IYM further argues that Côté's local layout requirements and additional constraints, each of which are identified using numeral 518, are one and the same. *Id.* at 33–34 (citing Ex. 1004, 5:30–34, Fig. 5; Ex. 1002 ¶ 78; Ex. 2013, 207:4–5; Ex. 2012 ¶ 77). IYM asserts that it would be improper for RPX to rely on the same element in Côté (i.e., local layout requirements 518 and additional constraints 518) to teach two separately identifiable features of the claimed invention—namely, the claimed "local process modifications" and "new local constraint distances." *Id.* at 34–35 (citing Ex. 2012 ¶ 78).

IYM further contends that RPX also relies on Côté's identification of problem areas in an attempt to compensate for Côté's purported failure to explain local layout requirements 518, how they are computed, or how they are used. PO Resp. 43 (citing Pet. 31). According to IYM, identifying problem areas does not play any role in the determination of Côté's local layout requirements 518 because only layout optimizer 520—not image analyzer 516—identifies problem areas. *Id.* at 43–44 (citing Ex. 1004, 5:30–31, Fig. 5; Ex. 2012 ¶¶ 89, 90). To support this argument, IYM directs us to Dr. Nagel's cross-examination testimony in which he purportedly confirms that Côté generates local layout requirements 518 prior to running layout optimizer 520. *Id.* at 44–45 (citing Ex. 2013, 239:17–240:2; Ex. 1004, 5:33–36; Ex. 2012 ¶ 91).

In its Reply, RPX counters that Côté's local layout requirements 518 are used to change the initial constraints imposed by design rules 505, and that change, which is calculated from the simulations received from process simulator 512, teaches the claimed "local process modifications." Pet. Reply 7 (citing Ex. 1004, 2:8–12, 2:45–47, 5:31–36, 6:9–17; Ex. 1002 ¶¶ 162–167), 8 (arguing that "the change (calculated from the simulation) is a 'local process modification' in the language of [independent] claim 1" (emphasis omitted)). RPX argues that IYM does not address Dr. Nagel's unrefuted testimony other than to argue that Côté's optimization process does not involve identifying problem areas. *Id.* at 7. RPX further argues that, when reading Côté, as a whole, Côté identifies problem areas before running layout optimizer 520 so that it can produce a new target layout addressing those problem areas. *Id.* at 15–16 (citing Pet. 22–23, 31–33; Ex. 1005, 2:38–50, 5:29–36).

In its Sur-Reply, IYM reiterates its argument that "local process modifications" and "new local constraint distances" are separately identifiable features of the claimed invention, and RPX cannot rely on Côté's local layout requirements and additional constraints, each of which is identified using numeral 518, to teach both of these claimed features. PO Sur-Reply 1–2 (citing Pet. Reply 23–24). IYM then argues that RPX's Reply mischaracterizes its position regarding these claimed features and then changes theories by arguing that

Côté's changes to the local layout requirements 518 constitute the claimed "local process modifications." *Id.* at 2–3 (citing Pet. 33, 50, 51; Pet. Reply 3, 23–24). IYM argues that RPX's purported new theory fails for the following three reasons: (1) at best, Côté discloses changes to the shapes of a design layout—not changes to constraints of the design layout; (2) Dr. Nagel's cross-examination testimony contradicts RPX's position that Côté's changes to the local layout requirements 518 constitute the claimed "local process modifications"; and (3) RPX's Reply is replete with confusing and contradictory statements regarding "local layout requirements," "additional constraints," "changes," and "distance." *Id.* at 3–5.

Based on the record developed during trial, we agree with RPX and its declarant, Dr. Nagel, that the changes to initial design rules 505 that result from running simulations on layout 510 amount to the claimed "local process modifications." Côté's process of generating and enhancing a design layout begins with inputting design 502 and ensuring that resulting layout 510 satisfies a set of initial design rules 505. Ex. 1004, 5:12–14. After running simulations on layout 510 using process simulator 512, image analyzer 516 analyzes simulated printed image 514 to identify problem areas, and then uses those problem areas to generate local layout requirements 518 to optimize latitude and/or layout characteristics (e.g., area). *Id.* at 5:30–33; *see also id.* at [57] ("The system . . . identifies problem areas in the simulated printed image that do not meet a specification."), Fig. 7 (illustrating problem areas in a printed image using highlighted white boxes). One example of a problem area is that the edges of the features may be spaced too closely together to cause potential bridging. *Id.* at 6:31–40, Fig. 7. This problem is addressed by creating a larger space between the features. *Id.* at 6:9–17, 6:31–40, Figs. 6, 7.

Based on these and other disclosures in Côté, RPX's declarant, Dr. Nagel, testifies that "Côté discloses simulating effects of manufacturing processes on . . . layout [510] to identify problem areas, from which local layout requirements are derived." Ex. 1002 ¶ 163 (citing Ex. 1004, 2:37–46, 5:17–29). Dr. Nagel further testifies that "Côté's 'local layout requirements [518]' are used to 'change' the initial constraint [imposed by design rules 505], and the change that is (calculated using the simulations) is a 'local process modification,'" as claimed. *Id.* ¶ 166. We credit Dr. Nagel's testimony in this regard because it is consistent with Côté's disclosure of the changes to initial design rules 505 that result from running simulations on layout 510.

Although IYM is correct that Côté identifies both local layout requirements and additional constraints using numeral 518 (Ex. 1001, 5:30–34), we do not agree with its argument that RPX relies on the same element in Côté to teach both the claimed "local process modifications" and "new local constraint distances." *See* PO Resp. 33–35; PO Sur-Reply 1–2. RPX relies on different teachings of Côté—albeit interrelated teachings—to account for these two claimed features. As we explain above, RPX relies on the changes to initial design rules 505 that result from running simulations on layout 510 to teach the claimed "local process modifications." As we explain below, RPX relies on Côté's additional constraints 518, which is the product of combining the changes identified above with the initial design rules 505, to teach the claimed "new local constraint distances." *See infra* Section II.B.4.c.

During cross-examination, Dr. Nagel was asked whether Côté's local layout requirements and additional constraints, each of which is identified using numeral 518, are the same thing. The relevant exchange is reproduced below.

> Q. Just to be clear, additional constraints 518 and local layout requirements 518 are the same thing; correct?
>
> A. Well, I guess it depends upon who you talk to. . . . I think the correct way of interpreting this is that the local layout requirements, which are the [local design rules], and the [global design rules] together form the new constraints 518 which feed into the layout optimizer [520]. So they've called—they're referring to the same thing by two different names, but elsewhere I think they mean different things by "layout requirements" than they do "additional constraints."
>
> Q. So you think the disclosure of Côté would be unclear to a person of ordinary skill?
>
> . . .
>
> [A.] I think it might cause a little confusion. I think once you sit down and study [Côté], you can figure out what they mean. But it's an unfortunate choice of words.

Ex. 2013, 183:20–184:14. We understand Dr. Nagel to testify that Côté's identification of both local layout requirements and additional constraints using numeral 518 was "an unfortunate choice of words," but nonetheless, when reading Côté, as a whole, one of ordinary skill in the art would have appreciated the subtle differences. This is consistent with general principles of obviousness, specifically that Figure 5 of Côté and its corresponding description of local layout requirements and additional constraints 518 "must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986); *see also In re Hedges*, 783 F.2d 1038, 1041 (Fed. Cir. 1986) (explaining that, when evaluating claims for obviousness, "the prior art as a whole must be considered").

We also do not agree with IYM's argument that Côté's identification of problem areas cannot be used to compute the claimed "local process modifications." *See* PO Resp. 43–45. IYM's argument in this regard is predicated on the notion that problem areas are not used to generate local layout requirements 518 because, when describing the generation and enhancement of a layout as illustrated in Figure 5 of Côté, the description of layout optimizer 520 is preceded by the following statement: "[n]ote that this further optimization can involve identifying problem areas in the layout as is illustrated in [Figure] 7." Ex. 1004, 5:30–36. When reading Côté, as a whole, it becomes clear that image analyzer 516 identifies problem areas and then uses those problem areas to generate local layout requirements 518, all of which occurs prior to layout optimizer 520 producing enhanced layout 522.

Côté's Abstract, which is produced below, provides context regarding the temporal significance of the processing steps illustrated in Figure 5 of Côté.

> During operation, the system receives a representation of a target layout for the integrated circuit . . . . *Next*, the system simulates effects of the manufacturing process on the target layout to produce a simulated printed image for

> the target layout. The system *then* identifies problem areas in the simulated printed image that do not meet a specification. *Next*, the system moves corresponding shapes in the target layout to produce a new target layout for the [IC].

Ex. 1004, [57] (emphases added), 2:41–50 (disclosing the same). Côté further discloses that "moving the corresponding shapes in the target layout involves applying relaxed rules to the problem areas of the target layout to improve process latitude." *Id.* at 3:1–4, 3:7–9 (disclosing the same). Applying this temporal significance to Côté's Figure 5, it follows that "problem areas" in layout 510 are identified and addressed (i.e., by image analyzer 516 using simulated image 514 to identify problem areas, and then using those problem areas to generate local layout requirements 518) prior to feeding additional constraints 518 into layout optimizer 520 to produce enhanced layout 522.

The cross-examination testimony of Dr. Nagel also supports our determination in this regard. When asked whether "local layout requirements [518] must be calculated prior to running . . . layout optimizer [520]," Dr. Nagel responded "Yes. They're calculated by . . . image analyzer [516]." Ex. 2013, 239:20–24. Dr. Nagel was then asked "[s]o . . . layout optimizer [520] does not calculate local layout requirements [518]; correct?" Dr. Nagel unequivocally responded "No." *Id.* at 239:25–240:2. We credit this testimony from Dr. Nagel because it is consistent with the temporal significance attributed to the processing steps illustrated in Figure 5 of Côté.

Lastly, we do not agree with IYM's argument that RPX's Reply presents a new theory as to how the teachings of Côté account for the claimed "local process modifications." *See* PO Sur-Reply 2–5. Contrary to

IYM's arguments, RPX consistently and repeatedly takes the position that Côté's changes to initial design rules 505 that result from running simulations on layout 510 teach the claimed "local process modifications." *Compare* Pet. 31–32, *with* Pet. Reply 7–8. As we explain above, this position has a sufficient basis in the teachings of Côté and it is supported by Dr. Nagel's testimony. Ex. 1004, 5:9–62, 6:9–17, 6:31–40, Figs. 5, 7; Ex. 1002 ¶¶ 162–167; Ex. 2013, 183:20–184:14, 239:17–240:2.

c. Côté Teaches "New Local Constraint Distances"

In its Patent Owner Response, IYM contends that Côté's additional constraints 518 do not constitute the claimed "new local constraint distances." PO Resp. 37. According to IYM, there are a number of reasons as to why the layout optimization illustrated in Figure 6 of Côté does not require "new local constraint distances." *Id.* As one example, IYM argues that the corresponding description of Figure 6 does not mention constraint distances at all. *Id.* at 38 (citing Ex. 1004, 5:65–6:28). As another example, IYM argues that, at his deposition, Dr. Nagel purportedly agreed that the layout optimization illustrated in Figure 6 could be obtained from the application of two additional constraints that are not constraint distances. *Id.* at 38. Relying on an annotated version of Figure 6 that is Exhibit 2018, IYM asserts that the two constraint distances are not "new local constraint distances," but rather they are two fixed positions. *Id.* at 38–39 (citing Ex. 1004, Fig. 6; Ex. 2012 ¶¶ 82, 83; Ex. 2013, 200:20–201:8, 210:22–211:10). IYM also argues that Exhibit 2019 represents Dr. Nagel's own depiction of Figure 6, but the hypothetical additional constraint d1 he inserted into this figure is not supported by the teachings of Côté. *Id.* at 39–40 (citing Ex. 2012 ¶ 84; Ex. 2013, 254:12–255:6; Ex. 2019).

Next, IYM contends that Côté's additional constraints 518 are not obtained "by combining . . . local process modifications with constraint distances in [a] system of initial constraints," as recited in independent claim 1. PO Resp. 40 (citing Ex. 1004, 5:30–34). According to IYM, Dr. Nagel purportedly agreed that Côté does not explain how to compute additional constraints 518. *Id.* at 40–41 (citing Ex. 2012 ¶ 85; Ex. 2013, 191:13–19). Relying once again on an annotated version of Figure 6 that is Exhibit 2018, IYM asserts that the two additional constraints illustrated in this figure are not constructed from constraint distances, let alone "by combining . . . local process modifications with constraint distances in [a] system of initial constraints." *Id.* at 41 (citing Ex. 2012 ¶ 86; Ex. 2013, 211:18–24).

IYM further contends that Dr. Nagel's reading of independent claim 1 contradicts his testimony that Côté's additional constraints 518 constitute the claimed "new local constraint distances." PO Resp. 41–42. According to IYM, Dr. Nagel testified, at his deposition, that "combining said local process modifications with constraint distances in said system of initial constraints," as recited in independent claim 1, cannot be satisfied by adding an entirely new constraint to the system of initial constraints. *Id.* at 42 (citing Ex. 2013, 65:15–19). IYM asserts that RPX's reading of Côté is exactly what Dr. Nagel believes is not covered by the aforementioned "combining" limitation—namely, feeding additional constraints 518 into layout optimizer 520, in addition to the initial constraints derived from design rules 505. *Id.* (citing Pet. 29, 30, 34; Ex. 1002 ¶¶ 158, 159, 172; Ex. 2012 ¶ 87).

Lastly, IYM contends that RPX improperly relies on Dr. Nagel's testimony to recreate the challenged claims from Côté's inadequate disclosure. PO Resp. 42. According to IYM, Côté's disclosure is missing the entire method step of "constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints," as recited in independent claim 1. *Id.* at 42–43 (citing Ex. 2012 ¶ 88). IYM asserts that, contrary to precedent from the U.S. Court of Appeals for the Federal Circuit, RPX relies on Dr. Nagel's conclusory testimony, unsupported by documentary evidence, to fill the gaps in the teachings of Côté. *See id.* at 43 (first citing *Motorola*, 121 F.3d at 1473; and then citing *Zoltek Corp. v. United States*, 815 F.3d 1302, 1309–14 (Fed. Cir. 2016)).

In its Reply, RPX counters that Côté's additional constraints 518, which are constructed from the initial distances imposed by initial design rules 505 in a local area, as well as the local process modifications determined from running simulations on layout 510, teach the claimed "new local constraint distances." Pet. Reply 8 (citing Pet. 33–35; Ex. 1004, 2:10–12, 5:31–36, 6:9–17). RPX disagrees with IYM's primary argument that Côté's additional constraints 518 do not constitute the claimed "new local constraint distances" because they are not constructed in the manner required by independent claim 1. *Id.* at 11. RPX asserts that this argument ignores Côté's actual teachings and mischaracterizes Dr. Nagel's cross-examination testimony. *Id.*

RPX also disagrees with IYM's argument that Côté never explains how to compute additional constraints 518, nor does it explain how to compute their numerical values. Pet. Reply 11. RPX contends that a particular algorithm for computing numerical values is irrelevant because no specific algorithm is claimed. *Id.* RPX also argues that IYM fails to consider Côté, as a whole. *Id.* at 12. RPX further contends that, IYM's declarant, Dr. Bernstein conceded that a person of ordinary skill in the art would have known that "constraints" are "limits on geometry parameters of the layout object in the design layout." *Id.* (citing Ex. 2012 ¶ 49; Ex. 1027, 52:2–12). RPX then argues that Côté's constraints are consistent with this construction because they can impose minimum distances. *Id.* (citing Ex. 1004, 1:59–60). RPX asserts that, as explained in the Petition, Côté's description of "'additional constraints [518]' to address local layout requirements discloses an 'initial distance required by an initial constraint' and a 'modification' to that constraint distance to address local layout requirements." *Id.* (citing Pet. 33–34; Ex. 1002 ¶¶ 168–171).

Next, RPX acknowledges that both the Petition and Dr. Nagel cite to Figure 6 of Côté as informing the meaning of additional constraints 518. Pet. Reply 12 (citing Pet. 33–34; Ex. 1002 ¶ 171). RPX, however, disagrees with IYM's assertion that Figure 6 is not applicable to constraints because its corresponding description does not mention constraints at all. *Id.* According to RPX, a person of ordinary skill in the art reading Côté, as a whole, would have understood that Figure 6 illustrates optimizing a layout by using the additional constraints that modify the initial constraint distances. *Id.* at 13 (citing Pet. 33–34; Ex. 1002 ¶¶ 168–171).

RPX further contends that the theoretical alternatives IYM proposes to Dr. Nagel during his cross-examination testimony are irrelevant because a person of ordinary skill in the art would have understood that Côté teaches computing additional constraints 518 in the manner required by independent claim 1. Pet. Reply 13. RPX also disagrees with IYM's argument that RPX's reading of Côté somehow contradicts Dr. Nagel's belief as to what is required by independent claim 1. *Id.* at 14. According to RPX, Dr. Nagel testified that the method step of "combining . . . local process modifications with constraint distances in [a] system of initial constraints" cannot be satisfied by forming an entirely new constraint that is not constructed from an initial constraint. *Id.* RPX then reiterates its argument that Côté's additional constraints 518 are constructed by combining local process modifications determined from running simulations on layout 510 with the initial distances imposed by initial design rules 505 on the local area. *Id.* RPX argues that Dr. Nagel never said that an additional constraint constructed from an initial constraint does not satisfy independent claim 1 if that additional constraint is fed into an optimizer along with the initial constraint, and RPX asserts nothing in independent claim 1 excludes that possibility. *Id.*

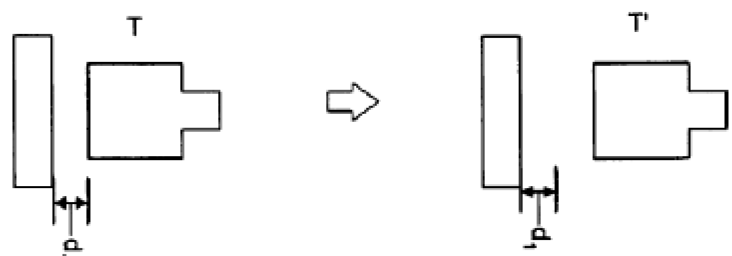
Lastly, RPX contends that IYM's reliance on the *Motorola* and *Zoltek* cases are inapposite. Pet. Reply 14. RPX argues that these two cases are distinguishable from the circumstances presented here because (1) *Motorola* was a case based on anticipation where the party solely relied on expert testimony to account for a limitation; and (2) *Zoltek* was a case that involved claims requiring a specific mathematical relationship missing from the asserted prior art. *Id.* (first citing *Motorola*, 121 F.3d at 1472–73; and then citing *Zoltek*, 815 F.3d at 1309–11). In contrast, RPX argues that it relies on specific teachings in Côté to account for the claimed "new local constraint distances," and it relies on Dr.

Nagel's supporting testimony to explain how a person of ordinary skill in the art would have understood these teachings in Côté. *Id.* at 14-15 (citing Pet. 8, 32–35).

In its Sur-Reply, IYM reiterates its argument that Côté discloses certain constraints, such as area constraints and fixed edge positions, which do not involve or require constraint distances. PO Sur-Reply 6 (citing PO Resp. 37–40; Ex. 1004, 5:30–33; Ex. 1027, 19:16–24, 255:4–10, 279:11–282:22). In addition, IYM reiterates its argument that Côté's additional constraints 518 are not obtained "by combining . . . local process modifications with constraint distances in [a] system of initial constraints," as recited in independent claim 1. *Id.* at 6–7 (citing PO Resp. 40–41). According to IYM, RPX's theory of unpatentability requires Côté to disclose explicitly the claimed "new local constraint distances." *Id.* at 7. IYM asserts that it is not enough that Côté's additional constraints 518 can be constraint distances. *Id.*

Based on the record developed during trial, we agree with RPX and its declarant, Dr. Nagel, that Côté's additional constraints 518, which are constructed by combining the initial distances imposed by design rules 505 together with the local process modifications determined from running simulations on layout 510, teaches the claimed "new local constraint distances." As background, Côté explains that IC layouts generally are created using a set of design rules that specify certain constraints, "such as minimum spacings" (i.e., constraint distances). Ex. 1004, 1:58–63. Côté, however, explains that using design rules that specify a minimum spacing between certain shapes may lead to sub-optimal layouts. *Id.* at 2:5–7. Côté states that "[i]t may be preferable to use a larger spacing between shapes whenever possible to improve 'process latitude.'" *Id.* at 2:10–12.

As we explain previously, when addressing how Côté teaches the claimed "local process modifications," Côté discloses making changes to initial design rules 505 that result from running simulations on layout 510. Ex. 1004, 5:12–33, 6:9–17, 6:31–40, Figs. 5, 7. These changes to the initial design rules 505 are used to construct additional constraints 518, which, in turn, are fed into layout optimizer 520 to "further optimize[]" layout 510. *Id.* at 5:31–36, Fig. 5. The portion of Figure 6 of Côté, reproduced below, serves as one example of the layout optimization illustrated in Figure 5 of Côté. *Id.* at 3:57–59, 5:66–67.



This portion of Figure 6, reproduced above, illustrates original target layout T with two features spaced a certain distance d1 apart and new target layout T' with the same two features "spaced further apart" that results in improved process latitude. *Id.* at 6:9–12. Based on this portion of Figure 6, we find that additional constraints imposed upon new target layout T' is a combination of the initial distance required by the original design rules (i.e., distance d1) together with the local process modifications determined from running simulations on original target layout T (i.e., the increase in distance between the two features that results in improved process latitude).

Based on these and other disclosures in Côté, RPX's declarant, Dr. Nagel, testifies that "Côté describes how the 'additional constraints [518]' are determined from the local process modifications and from initial constraints." Ex. 1002 ¶ 170; *see also id.* ¶ 171 (testifying that "Côté describes that these new local constraint distances are constructed based on both the initial distances required by an initial constraint in a local area, as well as the local process modifications determined from the simulating" (citing Ex. 1004, 2:10–12, 6:9–17)). Dr. Nagel further testifies that Côté's additional constraints 518 constitute "new 'constraint distances' that are applied to the local area of the layout, which are thus 'new local constraint distances,' in the language of [independent] claim 1." *Id.* ¶ 170. We credit Dr. Nagel's testimony in this regard because it is consistent with Côté's disclosure that additional constraints 518 are constructed by combining the initial distances imposed by design rules 505 together with the local process modifications determined from running simulations on layout 510.

We do not agree with IYM's argument that Côté's additional constraints 518 do not constitute the claimed "new local constraint distances" because Côté discloses some constraints that do not involve or require constraint distances. *See* PO Resp. 37–41; PO Sur-Reply 6–7. There is no dispute between the parties that the claim term "constraint" should be construed as "limits on geometry parameters of the layout objects in the design layout." *Compare* Pet. 28–29, *with* PO Resp. 14–17. During oral argument, the parties agreed that this claim term encompasses both minimum and maximum constraints. *See* Tr. 44:16–19 (explaining that independent claim 1 "does not limit the constraint distances to be a minimum or a maximum"), 45:1–10 (agreeing that the word "limits" referred to in the parties' agreed upon construction of the claim term "constraint" is not restricted to minimums or maximums), 99:13–15 (agreeing that independent claim 1 does not require minimum or maximum constraints).

As we explain above, Côté explains that IC layouts generally are created using a set of design rules that specify certain constraints, "such as minimum spacings" (i.e., constraint distances). Ex. 1004, 1:58–63. Indeed, the layout generation and enhancement process illustrated in Figure 5 of Côté provides one example of a constraint distance because it illustrates feeding additional constraints 518 into layout optimizer 520 to further optimize layout 510. *Id.* at 5:30–36, Fig. 5. Figure 6 of Côté provides another example of a constraint distance because it illustrates increasing the distance between two features in new target layout T' to improve process latitude. *Id.* at 6:9–12, Fig. 6. The teachings of Côté identified above are consistent with the parties' agreed upon construction of the claim term "constraint" because the constraint distances taught by Côté (e.g., additional constraints 518 or distance increase between the two features in new target layout T') places minimum or maximum limits on geometry parameters of layout objects in a design layout (e.g., layout 510 or new target layout T').

We also do not agree with IYM's argument that Dr. Nagel's cross-examination testimony contradicts his initial testimony that Côté's additional constraints 518 constitute the claimed "new local constraint distances." *See* PO Resp. 41–42. To support this argument, IYM directs us to the following statement elicited from Dr. Nagel during cross-examination: "The 'combining said local process modifications with constraint distances in said system of initial constraints' does not mean adding additional constraints that were heretofore not in the system of initial constraints." Ex. 2013, 65:15–19. Although somewhat difficult to decipher, we do not understand Dr. Nagel to take the position that the aforementioned "combining" method step cannot be satisfied by adding an entirely new constraint to the system of initial constraints, as asserted by IYM. PO Resp. 42. Instead, a reasonable reading of this cited testimony is that constructing additional constraints requires determining the initial constraints imposed upon local areas of the design layout. This reading is consistent with Dr. Nagel's testimony accompanying the Petition. *See* Ex. 1002 ¶¶ 168–172.

Regardless of how we decipher the portion of Dr. Nagel's cross-examination testimony identified above, IYM treats this cross-examination testimony as though it was articulated and relied on by RPX in the Petition. As we explain previously, we agree with RPX and Dr. Nagel that Côté's additional constraints 518, which are constructed by combining the initial distances imposed by design rules 505 together with the local process modifications determined from running simulations on layout 510, teach the claimed "new local constraint distances." We did not rely upon the aforementioned portions of Dr. Nagel's cross-examination testimony when determining whether the teachings of Côté account for this disputed limitation. Stated differently, the testimony elicited from Dr. Nagel during cross-examination does not undermine the evidence presented and developed by RPX in the Petition, or otherwise render Dr. Nagel's supporting testimony provided in the Declaration accompanying the Petition less persuasive.

Lastly, we do not agree with IYM's argument that RPX improperly relies on Dr. Nagel's testimony to fill gaps in the teachings of Côté. *See* PO Resp. 42–43. To support this argument, IYM directs us to the *Motorola* and *Zoltek* cases, both of which are distinguishable from the circumstances presented here. Beginning with *Motorola*, IYM relies on this case to support its assertion that we cannot rely on Dr. Nagel's testimony to supplant the teachings of Côté itself. *Motorola*, however, addressed a jury's invalidity findings and, in particular, whether an asserted prior art reference anticipated a claim of the involved patent. 121 F.3d at 1472. The Federal Circuit determined that the jury's verdict could not stand because it was impermissible to rely on an expert's conclusory testimony, unsupported by documentary evidence, to supplant the anticipatory disclosure of the asserted prior art reference itself. *Id.* at 1472–73. In contrast, the ground at issue here is one based on obviousness—not anticipation—over the teachings of Côté. A proper obviousness evaluation requires us to consider Dr. Nagel's testimony explaining the teachings of Côté relied on by RPX from the perspective of a person of ordinary skill in the art. *See Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1361 n.3 (Fed. Cir. 2008) ("What a prior art reference discloses or teaches is determined from the perspective of one of ordinary skill in the art.").

Turning to *Zoltek*, the Federal Circuit determined that certain claims in a reissue patent were not rendered obvious because the expert testimony was replete with examples of impermissible hindsight reconstruction. 815 F.3d at 1309–14. In contrast, apart from a few unsupported assertions, IYM does not explain adequately how Dr. Nagel's testimony is distorted by hindsight or how it is based on ex post reasoning. Contrary to IYM's assertions, there is no need for Dr. Nagel to recreate the entire method step of "constructing new local constraint distances by combining . . . local process modifications with constraint distances in [a] system of initial constraints," as recited in independent claim 1. As we explain previously, Côté teaches this method step because additional constraints 518 are constructed by combining the initial distances imposed by design rules 505 together with the local process modifications determined from running simulations on layout 510.

d. IYM's Remaining Arguments

In its Patent Owner Response, IYM contends that Côté lacks sufficient details to render the challenged claims obvious. PO Resp. 48. To support this argument, IYM directs us to Côté's teachings with respect to process simulator 512, image analyzer 516, and layout optimizer 520, along with the cross-examination testimony of RPX's declarant, Dr. Nagel. *Id.* at 48–52 (citing Ex. 1004, 5:17–19, 5:30–34, Figs. 5, 7; Ex. 2013, 106:8–108:9, 110:11–112:18, 177:13–178:11, 182:18–24, 189:2–190:5; Ex. 2012 ¶¶ 95–99). IYM then asserts that Côté adds nothing to the image analysis used in the prior art hotspot fixing procedure that was recognized by a provisional filing of the '012 patent. *Id.*

at 51 (citing Ex. 2014, 4–5[3]); *see also id.* at 52 (arguing that Côté "provides no technical advance over this prior art [hotspot fixing procedure]").

We do not agree that Côté's teachings lack sufficient detail to render the challenged claims obvious because, as we explain previously, Côté accounts for the limitations at issue, particularly when its teachings are viewed from the perspective of a person of ordinary skill in the art. To the extent IYM argues that the teachings of Côté cannot be used to render certain features of the challenged claims obvious because Côté is not directed to the same problem addressed by the '012 patent (i.e., fixing or eliminating hotspots in IC manufacturing), we also do not agree. *See* PO Resp. 48–52. It is well-settled that "[t]he use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned." *In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) (quoting *In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968)); *see also EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985) ("A reference must be considered for everything that it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect."). As a result, it is incumbent upon us to consider Côté for everything it teaches, regardless if it does not state explicitly that its optimization addresses hotspots in IC manufacturing.

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[3] All references to the page numbers in Exhibit 2014 refer to the page numbers inserted by IYM in the bottom, right-hand corner of each page.

IYM also contends that a person of ordinary skill in the art cannot provide the limitations purportedly missing from Côté—namely, the claimed "local process modifications" and "new local constraint distances." PO Resp. 53–54 (citing Ex. 2012 ¶ 102). Stated differently, IYM contends that RPX has not provided any evidence that a person of ordinary skill in the art would have found it obvious to add the limitations that Côté purportedly lacks. *Id.* at 55.

We do not agree with IYM's arguments in this regard because, as we explain previously, it is permissible for RPX to rely on the teachings of Côté together with the supporting testimony of Dr. Nagel in analyzing obviousness. *See Monsanto*, 878 F.3d at 1346–47. Indeed, a proper obviousness evaluation requires us to consider Dr. Nagel's testimony explaining the teachings of Côté from the perspective of a person of ordinary skill in the art. *See Sundance*, 550 F.3d at 1361 n.3. With this in mind, we agree with RPX's arguments and evidence demonstrating that Côté teaches the claimed "local process modifications" and "new local constraint distances." *See supra* Section II.B.4.a–c.

e. Remaining Limitations

In its Patent Owner Response, IYM does not address separately whether Côté teaches the remaining limitations of independent claim 1. *See generally* PO Resp. 30–57. We have reviewed RPX's explanations and supporting evidence as to how Côté teaches these remaining limitations, and we agree with and adopt RPX's analysis. *See* Pet. 23–31, 35–38.

e. Summary

In summary, RPX has demonstrated by a preponderance of the evidence that the subject matter of independent claim 1 would have been obvious over the teachings of Côté.

5. Claims 2 and 3

Claim 2 depends from independent claim 1, and recites "wherein the layout received is organized in a single level." Ex. 1001, 8:36–37. Dependent claim 3 also depends from independent claim 1, and further recites "wherein the layout received is organized in a hierarchical data structure." *Id.* at 8:38–39.

In its Petition, RPX contends that a person of ordinary skill in the art would have understood that the claim term "single level" refers to a flat data structure. Pet. 58 (citing Ex. 1001, 3:6–10; Ex. 1002 ¶ 253). RPX also contends that a person of ordinary skill in the art would have understood that there are two well-known types of data structures for organizing data—namely, (1) a flat (single level) data structure; and (2) a hierarchical (nested) data structure. *Id.* (citing Ex. 1002 ¶ 254). For example, RPX asserts that Graphic Design System and Caltech Intermediate Form were well-known layout formats that could be both flat and hierarchical. *Id.* According to RPX, a person of ordinary skill in the art would have appreciated the merits of both formats, depending on his/her goals or priorities for a given implementation, and would have used well-known criteria to make a selection. *Id.* at 58–59 (citing Ex. 1002 ¶ 255).

RPX further contends that a person of ordinary skill in the art would have found it obvious for Côté's layout 510 to be either a flat or hierarchical layout format, and would have recognized the selection of one over the other as a simple matter of design choice. Pet. 59 (citing Ex. 1002 ¶ 256). RPX argues that, even if a person of ordinary skill in the art would not have understood Côté to teach these layout formats, it would have been a conventional, expected, and obvious way for a person of ordinary skill in the art to format Côté's layout 510. *Id.*

In its Patent Owner Response, IYM does not address separately whether Côté teaches the limitations of dependent claims 2 and 3. *See generally* PO Resp. 30–62. We have reviewed RPX's explanations and supporting evidence as to how Côté teaches these limitations, and we agree with and adopt RPX's analysis. *See* Pet. 38, 58–59. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claims 2 and 3 would have been obvious over the teachings of Côté.

6. Claim 5

Claim 5 depends from independent claim 1, and recites "wherein the step of constructing initial constraints is accomplished using information comprising coordinates of said layout objects, design rules and circuit requirements." Ex. 1001, 8:44–47.

In its Petition, RPX directs us to its explanation and supporting evidence as to how Côté teaches constructing initial constraints imposed by design rules 505 in the context of independent claim 1. Pet. 38. RPX also contends that Côté teaches this limitation because it discloses constructing initial constraints with layout object coordinate information. *Id.* at 38–39 (citing Ex. 1004, 1:58–61, 2:1–4, 2:6–7, 2:41–44, Fig. 6; Ex. 1002 ¶¶ 189–192). Next, RPX contends that the '012 patent does not define circuit requirements nor does it disclose receiving circuit requirements. *Id.* at 39 (citing Ex. 1001, 3:5–11, 3:16–17, 3:36–37). Instead, RPX argues that the '012 patent merely discloses that constructing initial constraints from circuit requirements involves considering the geometries of layout objects in setting constraints based on circuit requirements. *Id.* (citing Ex. 1001, 3:36–42). RPX then argues that, to the extent initial constraints from circuit requirements require consideration of electrical characteristics, Côté teaches this limitation because it discloses determining "capacitance and resistance of wires" and producing "netlist" files that include "resistance and capacitance parameters." *Id.* at 40 (quoting Ex. 1004, 4:46–59). According to RPX, Côté's layout with built-in electrical characteristics produces the system of initial constraints required by dependent claim 5. *Id.* (citing Ex. 1002 ¶¶ 193, 194).

In its Patent Owner Response, IYM does not address separately whether Côté teaches the limitation of dependent claim 5. *See generally* PO Resp. 30–62. We have reviewed RPX's explanations and supporting evidence as to how Côté teaches this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 38–40. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 5 would have been obvious over the teachings of Côté.

7. Claim 13

Claim 13 depends from independent claim 1, and recites "wherein the system of initial constraints comprises linear constraints comprising minimal width, minimal space, minimal overlap, minimal enclosure, minimal extension, and fixed size." Ex. 1001, 9:16–19.

In its Petition, RPX contends that the claimed "linear constraints" are basic components of standard design rules that are well-known in the art. Pet. 59 (citing Ex. 1002 ¶¶ 257–262). RPX further argues that Côté teaches this limitation because it discloses that IC layouts generally are created using a set of design rules that specify certain constraints, "such as minimum spacings or minimum line widths" and a "fixed" layout area. *Id.* (quoting Ex. 1004, 1:58–64, 5:44–46). RPX asserts that a person of ordinary skill in the art would have understood that all the claimed "linear constraints" are part of Côté's "initial constraints" imposed by design rules 505 and were disclosed in standard design rules long before the '012 patent. *Id.* at 59–60 (citing Ex. 1002 ¶¶ 260–262).

In its Patent Owner Response, IYM does not address separately whether Côté teaches the limitation of dependent claim 13. *See generally* PO Resp. 30–62. We have reviewed RPX's explanations and supporting evidence as to how Côté teaches this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 38, 59–60. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 13 would have been obvious over the teachings of Côté.

8. Claim 14

Claim 14 depends from independent claim 1, and recites "wherein the step of enforcing new local constraint distance comprises applying a heuristic search procedure." Ex. 1001, 9:20–22.

In its Petition, RPX contends that, unlike optimization, "a heuristic search procedure" may not generate an optimal outcome. Pet. 40 (citing Ex. 1002 ¶¶ 196–198). RPX argues that a person of ordinary skill in the art would have known that heuristic solutions, as recognized by Chen's "single-error removal procedure" disclosed in the '012 patent, are alternatives to optimization. *Id.* (citing Ex. 1001, 4:49). Relying on the testimony of Dr. Nagel, RPX argues that heuristic procedures were well-known in the art of computer-implemented IC layouts. *Id.* (citing Ex. 1002 ¶ 198). RPX asserts that a person of ordinary skill in the art would have recognized that using a heuristic search procedure to enforce a new local constraint distance in lieu of Côté's optimization would have been a matter of design choice. *Id.*

In its Patent Owner Response, IYM contends that Côté does not teach the claimed "heuristic search procedure." PO Resp. 58. IYM argues that Côté discloses layout optimizer 520, but does not provide any details regarding its structure or operation. *Id.* (citing Pet. 7, 36, 43, 53; Ex. 1002 ¶¶ 179, 200, 228; Ex. 2013, 215:13–21). In addition, IYM argues that RPX's declarant, Dr. Nagel, purportedly agreed that Côté does not teach the claimed "heuristic search procedure" because, during his deposition, he stated that "[n]owhere in . . . the Côté patent is there a description of a heuristic search procedure, no." *Id.* (quoting Ex. 2013, 214:25–215:2) (citing Ex. 2012 ¶ 107).

IYM further contends that it would not have been obvious to substitute optimization performed by Côté's layout optimizer 520 with a heuristic search procedure. PO Resp. 58. According to IYM, the only evidence that might support such a conclusion for obviousness comes from the '012 patent itself. *Id.* at 59 (citing Pet. 40; Ex. 2012 ¶ 108). IYM argues that the '012 patent's own disclosure cannot support such a conclusion of obviousness because the disclosure in question is found in the description of the preferred embodiment of the invention—not in the background section. *Id.* at 59–60.

Lastly, IYM disagrees with RPX's contention that substituting a heuristic search procedure for the optimization performed by Côté's layout optimizer 520 would have been a matter of design choice. PO Resp. 60. IYM reiterates that Côté does not mention heuristic search procedures, but rather relies on well-known optimization methods to address problems formulated in terms of linear constraints. *Id.* IYM argues that the Petition does not cite to a single piece of evidence outside the '012 patent that would have provided the necessary motivation for a person of ordinary skill in the art to use a heuristic search procedure in lieu of the optimization performed by Côté's layout optimizer 520. *Id.* at 61. IYM recognizes that Dr. Nagel's supporting testimony references Allan as teaching a heuristic search procedure, but IYM asserts that Allan is not part of the instituted grounds in this proceeding, nor did Dr. Nagel explain how or why a person of ordinary skill in the art would have combined the teachings of Côté with those of Allan. *Id.* (citing Ex. 1015; Ex. 2012 ¶ 111).

In its Reply, RPX contends that IYM mischaracterizes its argument regarding how Côté renders dependent claim 14 obvious. Pet. Reply 25. RPX argues that it did not rely on any statement in the '012 patent for motivation to use heuristic search procedures in Côté, but rather it relied on the fact that using such procedures was a known design choice for layout optimization, as evidenced by Allan. *Id.* (citing Pet. 40; Ex. 1002 ¶ 198). Contrary to IYM's assertions, RPX argues that it is permissible for it to rely on the teachings of Allan, even though Allan is not part of the instituted grounds in this proceeding, because it serves as evidence of the general background knowledge of a person of ordinary skill in the art. *Id.*

In its Sur-Reply, IYM contends that RPX's argument that heuristic search procedures were well-known in the prior art is not enough for purposes of demonstrating obviousness. PO Sur-Reply 9. IYM argues that RPX cannot rely on the conclusory testimony of Dr. Nagel to support its argument that using a heuristic search procedure "would have been a matter of design choice." *Id.* at 10. IYM also argues that RPX cannot hide behind the fact that Allan is evidence of the general background knowledge of a person of ordinary skill in the art to avoid providing the explanation and evidentiary support that RPX would have been obligated to provide if Allan was part of the instituted grounds in this proceeding. *Id.*

Based on the record developed during trial, we agree with RPX that heuristic search procedures were old and well-known in the art, and a person of ordinary skill in the art would have recognized that such a procedure was a viable substitute for the optimization performed by Côté's layout optimizer 520. We begin our analysis by noting that dependent claim 14 does not require a specific heuristic search procedure because it simply states, in relevant part, "a heuristic search procedure." Ex. 1001, 9:21–22. Outside of dependent claim 14, the word "heuristic procedures" appears in the specification of the '012 patent only once. For convenience, the relevant portion of the specification is reproduced below.

> In another preferred embodiment, the violations to local constraints are removed one at a time using *heuristic procedures*. For example, the single error removal procedure described by Zhan Chen in "Layout and Logic Techniques for Yield and Reliability Enhancement", Ph.D. Thesis, University of Massachusetts Amherst, 1998, can be applied to fix isolated violations. It is

> particularly useful when processing hotspots are few.

Id. at 4:47–54 (emphasis added). This portion of the specification indicates that Chen's "single error removal procedure," which is admitted prior art to the '012 patent regardless of the fact the disclosure cited above appears in the detailed description, is a heuristic search procedure that is capable of being used to remove violations to local constraints in an IC layout. The specification does not include any other discussions of heuristic search procedures, examples of what those might be, or how they operate in the context of the claimed invention.

Based on the aforementioned disclosure in the specification of the '012 patent, we agree with RPX and Dr. Nagel that heuristic search procedures were old and well-known in the art of computer-implemented IC layout, as evidenced by Chen's "single error removal procedure." Pet. 40; Ex. 1002 ¶ 198. Taking this general background knowledge of one of ordinary skill in the art, we agree with RPX that it would have been a matter of design choice to substitute the optimization performed by Côté's layout optimizer 520 with a heuristic search procedure, such as Chen's "single error removal procedure." *See* Pet. 40. The evidence of record suggests that implementing Chen's "single error removal procedure" in a computer-implemented IC layout, as taught by Côté, would not have been uniquely challenging or otherwise beyond the skill level of an ordinary skilled artisan. *See Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 418). The record before us does not include credible evidence to the contrary.

We do not agree with IYM's argument that the '012 patent's disclosure regarding Chen's "single error removal procedure" cannot be treated as admitted prior art because this disclosure is found in the detailed description section of the '012 patent—not in the background or prior art section. *See* PO Resp. 59–60. It is well settled that admissions in a specification regarding prior art are not limited to a particular section of the specification. *See, e.g., PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1362 (Fed. Cir. 2007) ("Admissions in the specification regarding the prior art are binding on the patentee for purposes of a later inquiry into obviousness."); *In re Nomiya*, 509 F.2d 566, 571 (CCPA 1975) (holding applicant's labeling of two figures in the application drawings as "prior art" to be an admission that what was pictured was prior art relative to applicant's improvement). Nevertheless, during oral argument, when questioning IYM's counsel as to how Chen should be treated in the context of an obviousness evaluation of dependent claim 14, IYM's counsel stated, "to be clear, Chen is prior art." Tr. 73:7–15. In our view, this statement is an admission that Chen qualifies as admitted prior art and, therefore, is binding on IYM in this obviousness inquiry. *See Riverwood Int'l Corp. v. R.A. Jones & Co.*, 324 F.3d 1346, 1354 (Fed. Cir. 2003) ("Valid prior art may be created by the admissions of the parties.").

There is another reason we agree with RPX that heuristic search procedures were old and well-known in the art and, a person of ordinary skill in the art would have recognized that such a procedure is a viable substitute for the optimization performed by Côté's layout optimizer 520. When addressing dependent claim 14, Dr. Nagel testifies that Allan's "heuristic approach to adjusting a layout to account for local conditions" serves as evidence that heuristic search procedures are old and well-known in the art of IC layouts. Ex. 1002 ¶ 198 (citing Ex. 1015). Allan, which is titled "Computer-Aided Design of Integrated Circuits and Systems," was published in November 1992 and, therefore, qualifies as prior art to the '012 patent. Ex. 1015, Title page. Allan discloses that its "LocDes Program" "uses a heuristic algorithm that makes adjustments iteratively such that changes in layout geometry occur in a number of small steps." *Id.* at 1356.

Although IYM is correct that Allan was not part of the instituted grounds in this proceeding (PO Resp. 61; PO Sur-Reply 10), it is still incumbent upon us to consider its evidentiary value. The Federal Circuit has recognized that evidence submitted with the Petition may be considered to demonstrate the knowledge that one of skill in the art "would bring to bear in reading the prior art identified as producing obviousness." *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015); *see also Randall Mfg. v. Rea*, 733 F.3d 1355, 1362–63 (Fed. Cir. 2013) (emphasizing that additional prior art references or evidence are not for the purpose of changing the prior art combination that forms the basis of the asserted ground, but rather are merely for the purpose of providing evidence of the state of the art, including the general background knowledge of a person of ordinary skill in the art). Here, we view Allan, particularly its disclosure of using a heuristic algorithm in the context of computer-aided design of ICs, to fall within the purview of permissible evidence we may consider in our obviousness evaluation of dependent claim 14. Upon considering this evidence, we agree with RPX that it would have been a matter of design choice to substitute the optimization performed by Côté's layout optimizer 520 with a heuristic search procedure, such as the heuristic algorithm used by Allan's LocDes Program. *See* Pet. 40; Ex. 1002 ¶ 198; Ex. 1015, 1356.

In summary, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 14 would have been obvious over the teachings of Côté and the general background knowledge of one of ordinary skill in the art.

C. Obviousness Over the Combined Teachings of Côté and Bamji

RPX contends that claims 1–3, 5, 10, 11, and 13 of the '012 patent are unpatentable under § 103(a) over the combined teachings of Côté and Bamji. Pet. 41–60. RPX explains how this proffered combination teaches or suggests the subject matter of each challenged claim, and provides reasoning as to why one of ordinary skill in the art would have been prompted to modify or combine the teachings of these references. *Id.* RPX also relies on the Declaration of Dr. Nagel to support its positions. Ex. 1002 ¶¶ 200–263. In its Patent Owner Response, IYM contends that Bamji does not remedy the deficiencies in the teachings of Côté identified above in the ground based on obviousness over Côté alone. PO Resp. 62–64. IYM relies upon the Declaration of Dr. Bernstein to support its positions. Ex. 2012 ¶¶ 113–115.

We begin our analysis with a brief overview of Bamji, and then we address the parties' contentions with respect to the claims at issue in this asserted ground.

1. Bamji Overview

Bamji generally relates to the field of computer aided design and the analysis of structural systems, such as ICs. Ex. 1005, 1:11–13. In particular, Bamji discloses methods and systems for optimizing performance criteria, such as fabrication yield for ICs. *Id.* at 1:13–15. As background, Bamji discloses that conventional methods for improving yield fall into the following two categories: (1) layout topology is changed to improve yield; and (2) layout topology is fixed. *Id.* at 1:44–65. These methods, however, cannot be extended to other performance objectives. *Id.* at 1:66–2:1. According to Bamji, "[t]his problem of simultaneous optimization of multiple criteria is especially difficult to solve." *Id.* at 2:7–8.

Bamji solves this and other problems by providing a method, system and product "that guarantees an optimized yield for an [IC]." Ex. 1005, 2:21–23. The method and system "provide optimized yield for a fixed size IC, or alternatively, provide the maximum number of good IC's per wafer by increasing the size of the IC." *Id.* at 2:23–26. The method and system also "may be used to simultaneously optimize any number of performance criteria that have convex cost functions." *Id.* at 2:26–29. Bamji further discloses that its mathematical models "describe[] . . . performance criteria for the IC, such as defect probabilities for yield, power consumption, cross-talk delay, and the like," with each model relying on "spacing between layout objects." *Id.* at 2:57–62.

Figure 1 of Bamji, reproduced below, illustrates a system for optimizing fabrication yield in accordance with one embodiment. Ex. 1005, 4:38–40.

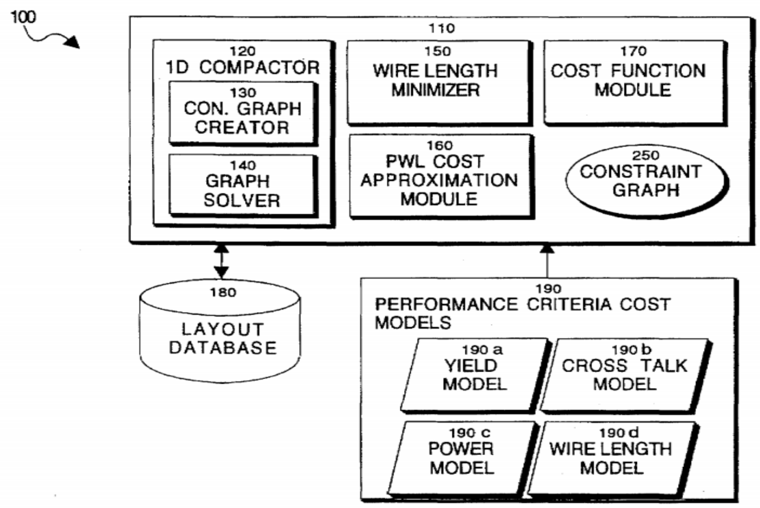

FIGURE 1

Figure 1, reproduced above, illustrates computer aided design system 100. Ex. 1005, 5:6–8. Computer aided design system 100 includes, among other things, compactor 120 that contains constraint graph creator 130 and graph solver 140. *Id.* at 5:43–44. Constraint graph creator 130 "reads a structural description of an [IC] from the layout database 180 and creates a constraint graph 250" (not illustrated in Fig. 1) using conventional techniques. *Id.* at 5:44–49. Graph solver 140 compacts constraint graph 250, "thereby produc[ing] a dimensionally minimized layout of the [IC]." *Id.* at 5:50–52.

2. Claim 1

In its Petition, RPX relies on essentially the same analysis discussed above in the ground based on obviousness over Côté alone to teach all the limitations of independent claim 1. Pet. 48–54 (citing Ex. 1002 ¶¶

210, 211). RPX also argues that the teachings of Bamji may be used to supplement the teachings of Côté to account for certain limitations of independent claim 1—namely, both "constructing" steps, the "enforcing" step, the "updating" step, and the "whereby" clause. *Id.* (citing Ex. 1005, 2:47–49, 5:25–36, 8:6–42, 20:40–41, Figs. 5a, 5b). In particular, with respect to the "whereby" clause, RPX asserts that Bamji teaches this limitation because it optimizes a constraint graph for yield and other performance criteria. *Id.* at 54 (citing Ex. 1005, 2:57–62). Relying on the testimony of Dr. Nagel, RPX asserts that one of ordinary skill in the art would have understood that the combined teachings of Côté and Bamji produce a new layout that has increased yield and performance. *Id.* (citing Ex. 1002 ¶ 234).

Turning to the rationale to combine the teachings of Côté and Bamji, RPX contends that, although Côté teaches optimization, it does not teach a particular optimization technique. Pet. 43 (citing Ex. 1002 ¶ 200). Bamji, however, teaches an optimization technique that simultaneously optimizes multiple performance objectives, as opposed to an approach that merely optimizes yield. *Id.* at 44 (citing Ex. 1005, 2:6–7, 2:28–30, 2:57–62). Relying on the testimony of Dr. Nagel, RPX asserts that one of ordinary skill in the art would have understood that Bamji's constraint graph optimization technique would be well-suited for Côté's layout optimizer 520. *Id.* (citing Ex. 1002 ¶¶ 201, 202). RPX argues that one of ordinary skill in the art would have been motivated to use Bamji's constraint graph optimization technique with Côté's layout optimizer 520 to provide simultaneous optimization of multiple performance criteria. *Id.* (citing Ex. 1002 ¶ 202). Stated differently, RPX argues that, although one of ordinary skill in the art would have recognized that optimizing for yield would be important, as taught by Côté, it also would have been desirable to optimize for IC performance like power consumption, cross-talk, wire length, and the like, as taught by Bamji. *Id.* Lastly, RPX asserts that one of ordinary skill in the art would have appreciated that the teachings of Côté and Bamji are compatible, and then reiterates that Bamji's constraint graph optimization technique could be used as the specific form of optimization employed by Côté's layout optimizer 520. *Id.* at 44–45 (citing Ex. 1002 ¶ 203).

In its Patent Owner Response, IYM contends that Bamji does not remedy Côté's purported failure to teach "computing local process modifications" and "constructing new local constraint distances by combining said local process modifications with constraint distances in [a] system of initial constraints," as recited in independent claim 1. PO Resp. 62 (citing Ex. 2012 ¶ 113). IYM argues that Bamji teaches conventional optimization techniques using only global constraints—not local constraints. *Id.* at 62–63 (citing Ex. 1005, 8:24–26, 12:26–28). To support this argument, IYM directs us to various excerpts of Dr. Nagel's cross-examination testimony, where he purportedly confirmed that Bamji only relies on global design rules. *Id.* at 63 (citing Ex. 1002 ¶ 205; Ex. 2013, 220:9–13, 221:25–222:2, 225:7–13; Ex. 2012 ¶ 14). IYM then asserts that, because Bamji only applies global design rules, it cannot remedy Côté's failure to teach the claimed "local process modifications" and "new local constraint distances." *Id.*

As we explain above in the ground based on obviousness over Côté alone, Côté teaches the claimed "local process modifications" and "new local constraint distances." *See supra* Section II.B.4.a–e. Consequently, there are not deficiencies with respect to these claim features in the teachings of Côté for Bamji to remedy. To the extent IYM argues that RPX cannot rely on Bamji to teach the claimed "new local constraint distances" because Bamji only applies global design rules, this argument ignores or fails to appreciate RPX's reliance on the teachings of Côté. *See* PO Resp. 62–64. As we explain previously, Côté's additional constraints 518, which are constructed by combining the initial distances imposed by design rules 505 together with the local process modifications determined from running simulations on layout 510, teaches the claimed "new local constraint distances." *See supra* Section II.B.4.c. In its ground based on obviousness over the combined teachings of Côté and Bamji, RPX contends that, when Bamji's constraint graph optimization technique is implemented by Côté's layout optimizer 520, Bamji's constraint graph would be modified based on Côté's additional constraints 518. Pet. 50 (citing Ex. 1002 ¶ 222). At no point in this asserted ground does RPX argue that Bamji, by itself, teaches the claimed "new local constraint distances." *See id.* at 50–51.

We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté and Bamji account for the limitations of independent claim 1, as well as RPX's reasoning as to why one of ordinary skill in the art would have been prompted to modify their respective teachings, and we agree with and adopt RPX's analysis. *See* Pet. 43–45, 48–54. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of independent claim 1 would have been obvious over the combined teachings of Côté and Bamji.

3. Claims 2, 3, and 13

RPX relies on the same analysis discussed above in the ground based on obviousness over Côté alone to teach the limitations of dependent claims 2, 3, and 13. Pet. 55, 58–60. In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté and Bamji account for the limitations of dependent claims 2, 3, and 13. *See generally* PO Resp. 62–64. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté and Bamji account for these limitations, and we agree with and adopt RPX's analysis. *See* Pet. 55, 58–60. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claims 2, 3, and 13 would have been obvious over the combined teachings of Côté and Bamji.

4. Claim 5

In its Petition, RPX directs us to its explanation and supporting evidence as to how the combined teachings of Côté and Bamji account for constructing initial constraints using design rules in the context of independent claim 1. Pet. 55. RPX contends that Bamji's layout database 180 includes structural descriptions of an IC, layout objects, and the coordinates of the layout objects, all of which are used to build a constraint graph. *Id.* (citing Ex. 1005, 5:18–31, 8:7–10, 8:23–26). RPX then argues that, to the extent the claimed "circuit requirements" are determined from geometries, Bamji teaches this limitation because it discloses setting initial constraints based on geometries of layout objects. *Id.* Alternatively, RPX argues that, to the extent the claimed "circuit requirements" require consideration of electrical characteristics, Bamji teaches this limitation because it provides for consideration of circuit requirements (e.g., power consumption) when constructing initial constraints. *Id.* at 56 (citing Ex. 1005, 6:11–15, 7:18–22; Ex. 1002 ¶ 242). RPX asserts that a person of ordinary skill in the art would have understood that, to make use of Bamji's power consumption model 190c, electrical characteristics would be considered in building its constraint graphs. *Id.* (citing Ex. 1002 ¶¶ 237–242).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté and Bamji account for the limitation of dependent claim 5. *See generally* PO Resp. 62–64. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté and Bamji account for this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 55–56. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 5 would have been obvious over the combined teachings of Côté and Bamji.

5. Claim 10

Claim 10 depends from independent claim 1, and recites "wherein the step of enforcing new local constraint distances comprises optimizing a predefined objective function for optimizing measurable performance of a layout, subject to said new local constraint distances." Ex. 1001, 8:66–9:3.

In its Petition, RPX contends that the Côté and Bamji combination would have used Bamji's constraint graph optimization technique and, as a result, this combination teaches the limitation of dependent claim 10. Pet. 56. RPX argues that Bamji discloses minimizing one or more "predefined" cost functions (i.e., a function of the "spacing between two layout objects"), including cost functions derived from performance models that include power consumption, wire length, cross-talk, etc. *Id.* (quoting Ex. 1005, 7:34–52) (citing Ex. 1005, 2:57–62, 3:1–15). RPX further argues that Bamji discloses that the cost functions account for the distances specified by the design rules. *Id.* (citing Ex. 1005, 8:23–30). RPX then asserts that, in the Côté and Bamji combination, a person of ordinary skill in the art would have understood that Côté's additional constraints 518 would have been combined with the initial constraints in Bamji's constraint graph to yield new enforceable constraints. *Id.* at 56–57.

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté and Bamji account for the limitation of dependent claim 10. *See generally* PO Resp. 62–64. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté and Bamji account for this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 56–57. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 10 would have been obvious over the combined teachings of Côté and Bamji.

6. Claim 11

Claim 11 depends from independent claim 1, and recites the following:

> wherein the step of enforcing new local constraint distances comprises receiving coefficients for an objective function selected from a group consisting of objective function for legalizing the layout with minimal changes from the original layout, objective function for minimizing, and objective function for minimizing the layout area, subject to said new local constraint distances.

Ex. 1001, 9:4–10.

In its Petition, RPX contends that dependent claim 11 is written in Markush format because it recites "selected from a group consisting of" and, therefore, the combined teachings of Côté and Bamji need only account for one of the listed objective functions to render this claim obvious. Pet. 57. RPX argues that both Côté and Bamji teach the claimed "objective function for minimizing the layout area" because they both teach compaction, and RPX further emphasizes Bamji's disclosure of receiving "coefficients for" an objective function. *Id.* (citing Ex. 1004, 2:62–64, 5:50–51; Ex. 1005, 5:51–53, 9:39–50, 15:53–57, Table 1; Ex. 1002 ¶ 250).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté and Bamji account for the limitation of dependent claim 11. *See generally* PO Resp. 62–64. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté and Bamji account for this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 57. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 11 would have been obvious over the combined teachings of Côté and Bamji.

D. Obviousness Over the Combined Teachings of Côté, Bamji, and Kroyan

RPX contends that claims 4 and 6–9 of the '012 patent are unpatentable under § 103(a) over the combined teachings of Côté, Bamji, and Kroyan. Pet. 60–68. In support of its contentions, RPX explains how this proffered combination teaches or suggests the subject matter of each challenged claim, and provides reasoning as to why one of ordinary skill in the art would have been prompted to modify the teachings of these references. *Id.* RPX also relies on the Declaration of Dr. Nagel to support its positions. Ex. 1002 ¶¶ 264–304. By virtue of their dependency, IYM contends that claims 4 and 6–9 include all the limitations of independent claim 1 and, therefore, these claims are patentable over the combined teachings of Côté, Bamji, and Kroyan for the same reasons discussed above with respect to the grounds based on obviousness over the teachings of Côté alone and the combined teachings of Côté and Bamji. PO Resp. 64–65.

We begin our analysis with a brief overview of Kroyan, and then we address RPX's contentions with respect to the claims at issue in this asserted ground.

1. Kroyan Overview

Kroyan generally relates to a system and method for designing ICs fabricated by a semiconductor manufacturing process and, in particular, to designing ICs to enhance manufacturability and improve yield. Ex. 1006, 1:22–28. Figure 3 of Kroyan, reproduced below, illustrates a method for IC design in accordance with one embodiment. *Id.* at 4:43–45.

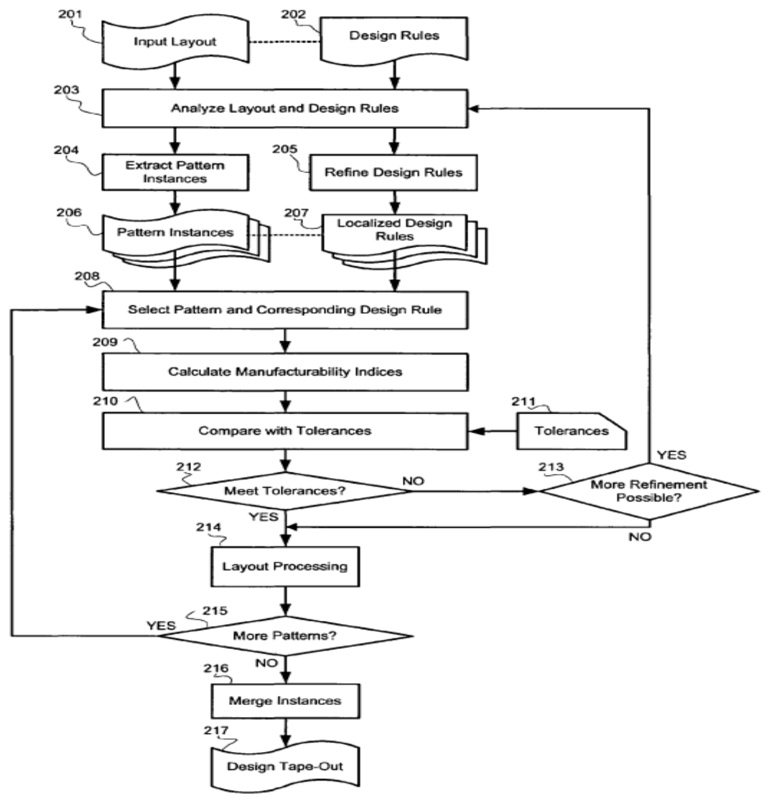

Figure 3

Figure 3 of Kroyan, reproduced above, illustrates that, at step 203, analysis engine receives input layout 201 and design rules 202. *Id.* at 5:63–66. The analysis engine evaluates the layout and design rules by determining distinct pattern types that "have different criticality leading to different manufacturability margin requirements." *Id.* at 6:4–7. In step 204, certain pattern instances 206 are extracted. *Id.* at 6:17–18. Similarly, at step 205, localized design rules are produced that correspond to each extracted pattern instance. *Id.* at 6:18–20. At step 208, each pattern instance and localized design rule is selected for an evaluation of manufacturability indices at step 209. *Id.* at 6:20–23. At step 210, the results of calculating the manufacturability indices are compared against past tolerances 211. *Id.* at 6:30–31. In step 212, if the results are within the tolerances, the selected design rules are suitable for the given pattern instances. *Id.* at 6:31–34. The process then proceeds to step 214, where the layout is processed according to these selected design rules. *Id.* at 6:34–35. At step 213, if more refinement is needed, the process returns to step 203 for further analysis. *Id.* at 6:35–39.

Figure 9 of Kroyan, reproduced below, illustrates a flow diagram of an intelligent analysis and optimization resolution enhancement technique in accordance with another embodiment. Ex. 1006, 4:62–64.

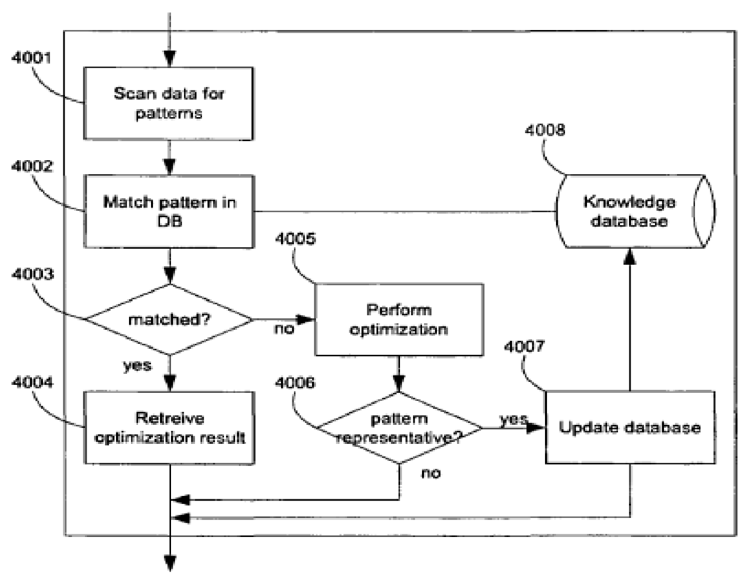

Figure 9

Figure 9 of Kroyan, reproduced above, illustrates that, at step 4001, the input design layout first is scanned and, at step 4002, the output layout patterns are compared against data stored in database 4008. *Id.* at 9:1–5. At step 4003, if a match is found, an optimization result is retrieved at step 4004. *Id.* at 9:6–7. At step 4005, if a match is not found, then a decision is made whether to store the results in the database at step 4006. *Id.* at 9:7–11. If the results are stored, database 4008 is updated at step 4007. *Id.* at 9:11–12.

2. Claim 4

Claim 4 depends from independent claim 1, and recites "wherein said description of manufacturing process comprises design rules, simulation models, equipment settings, material selections, and look-up data tables." Ex. 1001, 8:40–43.

In its Petition, RPX contends that the combined teachings of Côté, Bamji, and Kroyan account for this limitation because Côté discloses design rules, simulation models, equipment settings, and material selections, Bamji provides additional disclosures of design rules and simulation models, and Kroyan discloses the same features along with material selections. Pet. 64 (citing Ex. 1004, 5:12–14, 5:17–29; Ex. 1005, 6:11–15, 8:25–26; Ex. 1006, 5:62–66, 9:34–36, 9:41–46; Ex. 1002 ¶¶ 271, 272). Based on the disclosures in all three references, RPX argues that a person of ordinary skill in the art would have understood that physical models include material selections, such as the type of photoresist or etchant. *Id.* (citing Ex. 1002 ¶ 273). RPX further argues that Kroyan discloses receiving look-up data tables because it uses a knowledge database to evaluate a layout and "comput[e] local process modifications." *Id.* at 64–65 (citing Ex. 1006, 8:57–9:17, 10:46–58, 11:55–12:3; Ex. 1002 ¶¶ 274–279).

Turning to the rationale to combine the teachings of Côté, Bamji, and Kroyan, RPX contends that it would have been obvious to a person of ordinary skill in the art to combine the teachings of Côté and Bamji with those of Kroyan because Kroyan adds an efficiency to the optimization process by disclosing a database that stores both pattern instances for weak spots in a layout and previously-determined optimization techniques for addressing those weak spots. Pet. 62 (citing Ex. 1006, 9:1–14). According to RPX, if a given layout does not match a pattern instance, Kroyan discloses determining another optimization technique and storing the information regarding the layout change. *Id.* (citing Ex. 1006, 9:1–14, 11:55–12:3). RPX asserts that a person of ordinary skill in the art would have appreciated that Kroyan's knowledge database that stores layout patterns would improve the efficiency of the optimization technique taught by the combination of Côté and Bamji because the knowledge database would provide the opportunity to re-use previously determined optimization techniques for future layouts. *Id.* (citing Ex. 1002 ¶ 266). RPX also contends that a person of ordinary skill in the art would have recognized that Kroyan's approach for identifying weak spots in a design layout would be more efficient than evaluating a layout, as a whole, because Kroyan discloses evaluating the layout for weak spots at "discrete evaluation points." *Id.* (quoting Ex. 1006, 9:60–10:8) (citing Ex. 1002 ¶ 267).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté, Bamji, and Kroyan account for the limitation of dependent claim 4. *See generally* PO Resp. 64–65. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté, Bamji, and Kroyan account for this limitation, as well as RPX's reasoning as to why one of ordinary skill in the art would have been prompted to modify their respective teachings, and we agree with and adopt RPX's analysis. *See* Pet. 61–62, 64–65. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 4 would have been obvious over the combined teachings of Côté, Bamji, and Kroyan.

3. Claim 6

Claim 6 depends from independent claim 1, and recites "wherein calculating local process modification comprises detecting processing hotspots, evaluating process response variables in the neighborhood of said processing hotspots, and calculating local process modification values using a predetermined function of said process response variables." Ex. 1001, 8:48–53.

In its Petition, RPX contends that Kroyan teaches the claimed "detecting processing hotspots" because it discloses identifying weak spots in a design layout, such as those associated with placement error. Pet. 66 (citing Ex. 1006, 4:4–22, 7:26–40, 10:26–35; Ex. 1002 ¶¶ 281–283). RPX also contends that Kroyan teaches the claimed "evaluating process response variables in the neighborhood of said processing hotspots, and calculating local process modification values using a predetermined function of said process response variables" because Kroyan's weak spots are analyzed to determine "associated non-compliance properties," after which Kroyan "calculates functional relationships between non-compliant manufacturability parameters and layout parameters." *Id.* (quoting Ex. 1006, 10:26–35, 11:30–35) (citing Ex. 1002 ¶ 284). According to RPX, Kroyan discloses that these functional relationships are used to determine "possible combinations of layout modification instructions that have an influence on the non-compliant manufacturability parameter." *Id.* (quoting Ex. 1006, 11:44–54) (citing Ex. 1002 ¶ 285).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté, Bamji, and Kroyan account for the limitation of dependent claim 6. *See generally* PO Resp. 64–65. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté, Bamji, and Kroyan account for this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 65–66. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 6 would have been obvious over the combined teachings of Côté, Bamji, and Kroyan.

4. Claim 7

Claim 7 depends from independent claim 1, and recites "wherein local process modifications are calculated using simulation models at plurality of control points in the interaction region of a plurality of layout objects that are interrelated through constraints." Ex. 1001, 8:54–57.

In its Petition, RPX contends that Kroyan teaches this limitation because it discloses identifying weak spots in a design layout by evaluating manufacturability parameters at "discrete evaluation points." Pet. 67 (quoting Ex. 1006, 9:54–10:8) (citing Ex. 1002 ¶¶ 288, 289). RPX argues that Kroyan's "discrete evaluation points" relate to layout objects that are subject to constraints imposed by design rules because they are used to analyze a layout at a desired level of granularity. *Id.* (citing Ex. 1002 ¶¶ 290, 291). According to RPX, because the combination of Côté, Bamji, and Kroyan would incorporate Kroyan's approach for identifying weak spots in a design layout into Côté's approach for identifying problem areas in a design layout, the proffered combination teaches the limitation of dependent claim 7. *Id.* (citing Ex. 1002 ¶ 292).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté, Bamji, and Kroyan account for the limitation of dependent claim 7. *See generally* PO Resp. 64–65. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté, Bamji, and Kroyan account for this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 66–67. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 7 would have been obvious over the combined teachings of Côté, Bamji, and Kroyan.

5. Claim 8

Claim 8 depends from independent claim 1, and recites "wherein local process modifications are calculated from simulated local printability comprising edge placement error, light intensity during lithography exposure, and their derivatives from a plurality of layout objects that are interrelated through constraints." Ex. 1001, 8:58–62.

In its Petition, RPX contends that Kroyan teaches this limitation because it discloses printability characteristics, placement error, and light intensity during lithography exposure. Pet. 67 (citing Ex. 1006, 2:5–10, 6:42–47, 7:26–40, 9:41–46, 9:54–10:8, 11:44–54; Ex. 1002 ¶ 294). RPX asserts that a person of ordinary skill in the art would have understood that Kroyan's parameters, such as depth of focus and exposure latitude, amount to characteristic parameters of the lithography process. *Id.* at 67–68. RPX also contends that Kroyan teaches the claimed "derivatives." *Id.* at 68 (citing Ex. 1002 ¶ 297).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté, Bamji, and Kroyan account for the limitation of dependent claim 8. *See generally* PO Resp. 64–65. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté, Bamji, and Kroyan account for this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 67–68. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 8 would have been obvious over the combined teachings of Côté, Bamji, and Kroyan.

6. Claim 9

Claim 9 depends from independent claim 1, and recites "wherein the step of computing local process modification comprises searching a look-up data table." Ex. 1001, 8:63–65.

In its Petition, RPX contends that Kroyan teaches this limitation because, when addressing a design layout with problematic weak spots, Kroyan discloses using its knowledge database to retrieve an "associated remedial solution" and then providing that solution to an optimizer (e.g., Côté's layout optimizer 520). Pet. 68 (quoting Ex. 1006, 11:55–12:3) (citing Ex. 1006, 9:1–17, 10:46–58). According to RPX, Kroyan's "associated remedial solutions" amount to the "local process modifications," as recited in independent claim 1. *Id.* (citing Ex. 1002 ¶¶ 300–303). RPX argues that the combination of Côté, Bamji, and Kroyan teaches searching a "look-up table" because Kroyan's knowledge database may be used to compute the claimed "local process modifications." *Id.* (Ex. 1002 ¶ 304).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté, Bamji, and Kroyan account for the limitation of dependent claim 9. *See generally* PO Resp. 64–65. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté, Bamji, and Kroyan account for this limitation, and we agree with and adopt RPX's analysis. *See* Pet. 68. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 9 would have been obvious over the combined teachings of Côté, Bamji, and Kroyan.

E. Obviousness Over the Combined Teachings of Côté, Bamji, and Cobb

RPX contends that claim 12 of the '012 patent is unpatentable under § 103(a) over the combined teachings of Côté, Bamji, and Cobb. Pet. 69–72. In support of its contentions, RPX explains how this proffered combination teaches or suggests the subject matter of the challenged claim, and provides reasoning as to why one of ordinary skill in the art would have been prompted to modify the teachings of these references. *Id.* RPX also relies on the Declaration of Dr. Nagel to support its positions. Ex. 1002 ¶¶ 305–311. By virtue of its dependency, IYM contends that claim 12 includes all the limitations of independent claim 1 and, therefore, this claim is patentable over the combined teachings of Côté, Bamji and Cobb for the same reasons discussed above with respect to the grounds based on obviousness over the teachings of Côté alone and the combined teachings of Côté and Bamji. PO Resp. 64–65.

We begin our analysis with a brief overview of Cobb, and then we address RPX's contentions with respect to the claims at issue in this asserted ground.

1. Cobb Overview

Cobb generally relates to IC design and, in particular, to designing deep submicron ICs. Ex. 1007, 1:8–10. As background, Cobb discloses that optical proximity correction ("OPC") refers to modifying IC designs "to compensate for manufacturing distortions due to the relative proximity of edges in the design." *Id.* at 2:12–16. OPC also accounts for manufacturing distortions "introduced during chemical processing, such as resist etching and oxide etchings." *Id.* at 2:16–20. Cobb discloses two types of OPC: (1) model-based OPC; and (2) rule-based OPC. *Id.* at 2:28–29, 2:43–44. Model-based OPC predicts manufacturing distortions in a design layout and compensates for them at the design stage by operating on edge fragments. *Id.* at 2:29–32. Cobb, however, discloses that "[m]odel-based OPC can be very computationally intensive." *Id.* at 2:34. Rule-based OPC introduces a pre-determined alteration when a particular feature is encountered in a design layout. *Id.* at 2:44–46. Cobb, however, discloses that "[r]ule-based OPC . . . relies on the presumption that altering a particular feature with a predetermined change will improve the quality of the manufacturing design. [This] presumption does not always hold true." *Id.* at 2:50–53. According to Cobb, it would be desirable if both model-based OPC and rule-based OPC "could be selectively employed at a feature level in an efficient manner." *Id.* at 3:16–18.

Cobb seeks to achieve this objective by providing a method and apparatus for designing IC layouts composed of edge fragments by identifying and tagging certain properties of each edge fragment. Ex. 1007, 4:30–34. After an edge fragment has been identified and tagged, it can be controlled in various ways. *Id.* at 4:35–38. For instance, "a user can apply different types of . . . [OPC] to the tagged edge fragments, or view which edges in an IC layout have received certain tags." *Id.* at 4:38–42. Cobb discloses that its method and apparatus for designing IC layouts "may achieve performance advantages, for instance, by selectively applying OPC to only tagged edge fragments, resulting in a potentially significant time savings." *Id.* at 4:48–51.

2. Claim 12

Claim 12 depends from independent claim 1, and recites "tagging locations on a layer where enforcing said new local constraint distances are unsuccessful, and performing optimal process correction only on said tagged locations, whereby the processing time and data size of the mask layout is reduced." Ex. 1001, 9:11–15.

In its Petition, RPX contends that Cobb teaches this limitation because it discloses an approach for "selectively applying OPC to only tagged edge fragments, resulting in a potentially significant time savings." Pet. 71 (quoting Ex. 1007, 4:48–51). RPX argues that Cobb discloses identifying and tagging edge fragments of IC layouts that have specific properties indicative of "edge placement distortion due to the proximity of neighboring features." *Id.* (quoting Ex. 1007, 3:25–31) (citing Ex. 1007, 4:30–41). According to RPX, the combination of Côté, Bamji, and Cobb would include a step of performing OPC, as taught by Côté, and that OPC would be capable of using Cobb's selective tagging technique. *Id.* at 71–72. Stated differently, RPX asserts that, when Cobb's selective tagging technique is applied to the combination of Côté, Bamji, and Cobb in a manner that follows the optimization performed by Côté and Bamji, the edge fragments tagged would be those for which the enforcement of new local constraint distances were unsuccessful. *Id.* at 72 (citing Ex. 1002 ¶¶ 309–311).

Turning to the rationale to combine the teachings of Côté, Bamji, and Cobb, RPX contends that a person of ordinary skill in the art would have been motivated to combine the teachings of Côté and Bamji with those of Cobb because Côté discloses analyzing and adjusting a design layout using OPC to yield a new design layout. Pet. 70 (citing Ex. 1004, 3:16–22, 6:25– 28, 7:43–48). RPX argues that Cobb discloses achieving substantial performance advantages by identifying specific edge fragments at risk of manufacturing distortion and "selectively applying OPC to only tagged edge fragments." *Id.* (quoting Ex. 1007, 4:43–51). According to RPX, a person of ordinary skill in the art would have appreciated the advantages of implementing Côté's OPC using Cobb's selectively tagging technique in order to gain the performance advantages or efficiencies taught by Cobb. *Id.* (citing Ex. 1004, 6:18–27; Ex. 1007, 4:51–65; Ex. 1002 ¶¶ 306, 307).

In its Patent Owner Response, IYM does not address separately whether the combined teachings of Côté, Bamji, and Cobb account for the limitation of dependent claim 12. *See generally* PO Resp. 64–65. We have reviewed RPX's explanations and supporting evidence as to how the combined teachings of Côté, Bamji, and Cobb account for this limitation, as well as RPX's reasoning as to why one of ordinary skill in the art would have been prompted to modify their respective teachings, and we agree with and adopt RPX's analysis. *See* Pet. 70–72. Accordingly, RPX has demonstrated by a preponderance of the evidence that the subject matter of dependent claim 12 would have been obvious over the combined teachings of Côté, Bamji, and Cobb.

F. Constitutional Challenge

IYM contends that the Supreme Court's decision in *Oil States Energy Services LLC v. Greene's Energy Group, LLC*, 138 S. Ct. 1365 (2018) was limited to addressing *Oil States*'s constitutional challenge that subjecting its patent to an *inter partes* review proceeding violates its right to a jury trial under the Seventh Amendment of the U.S. Constitution. PO Resp. 65. IYM noted that that Supreme Court emphasized that its *Oil States* decision "should not be misconstrued as suggesting that patents are not property for purposes of the Due Process Clause or the Takings Clause." *Id.* (quoting *Oil States*, 138 S. Ct. at 1379).

IYM contends that our exercise of jurisdiction to adjudicate the patentability of the '012 patent would violate its rights under the Takings Clause of the Fifth Amendment of the U.S. Constitution because this patent issued in November 2008, which was several years prior to the enactment of the America Invents Act ("AIA"). PO Resp. 65. According to IYM, the retroactive nature of this *inter partes* review proceeding underscores the unconstitutionality of the entire process. *Id.* IYM also argues that subjecting the '012 patent to an *inter partes* review proceeding "places a severe, disproportionate, and extremely retroactive burden on" IYM. *Id.* at 66 (quoting *E. Enters. v. Apfel*, 524 U.S. 498, 538 (1998)).

In its Reply, RPX contends that IYM does not offer any substantive analysis to support its argument that subjecting the '012 patent to an *inter partes* review proceeding violates IYM's rights under the Takings Clause. Pet. Reply 26. RPX further contends that IYM does not cite to any authority that would authorize the Board to determine that the "retroactive" application of the AIA is unconstitutional. *Id.*

We decline to consider IYM's constitutional challenge because "administrative agencies [generally] do not have jurisdiction to decide the constitutionality of congressional enactments." *Riggin v. Office of Senate Fair Emp't Practices*, 61 F.3d 1563, 1569 (Fed. Cir. 1995); *see also Harjo v. Pro-Football, Inc.*, 50 USPQ2d 1705, 1710 (TTAB 1999) ("[T]he Board has no authority . . . to declare provisions of the Trademark Act unconstitutional."), rev'd on other grounds, 284 F. Supp. 2d 96 (D.D.C. 2003). *But see Am. Express Co. v. Lunenfeld*, Case CBM2014-00050, slip op. at 9–10 (PTAB May 22, 2015) (Paper 51) ("[F]or the reasons articulated in *Patlex* [*Corp. v. Mossinghoff*, 758 F.2d 594 (Fed. Cir. 1985)], we conclude that covered business method patent reviews, like reexamination proceedings, comply with the Seventh Amendment.").

III. CONCLUSIONS

RPX has demonstrated by a preponderance of the evidence that (1) claims 1–3, 5, 13, and 14 are unpatentable under § 103(a) over the teachings of Côté; (2) claims 1–3, 5, 10, 11, and 13 are unpatentable under § 103(a) over the combined teachings of Côté and Bamji; and (3) claims 3, 4, and 6–9 are unpatentable under § 103(a) over the combined teachings of Côté, Bamji, and Kroyan; and (4) claim 12 is unpatentable under § 103(a) over the combined teachings of Côté, Bamji, and Cobb.

IV. ORDER

In consideration of the foregoing, it is

ORDERED that claims 1–14 of the '012 patent are held to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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APPENDIX D

Trials@uspto.gov | Paper No. 35
571-272-7822 | Entered: March 6, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RPX CORPORATION and ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

IYM TECHNOLOGIES LLC,
Patent Owner.

Case IPR2017-01888
Patent 7,448,012 B1

Before MICHAEL R. ZECHER, MINN CHUNG, and CARL L. SILVERMAN, *Administrative Patent Judges*.
SILVERMAN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In response to a Petition (Paper 1, "Pet.") filed by RPX Corporation and Advanced Micro Devices, Inc., (collectively "RPX"), we instituted an *inter partes* review of claims 1–11, 13, and 14 of U.S. Patent No. 7,448,012 B1 (Ex. 1001, "the '012 patent"). Paper 9 ("Dec. on Inst.").

During the trial, IYM Technologies LLC ("Patent Owner") filed a Response (Paper 17, "PO Resp."), to which RPX filed a Reply (Paper 23, "Pet. Reply"). With our authorization, IYM filed a Sur-Reply (Paper 27, "PO Sur-Reply"). A consolidated oral hearing with related Case IPR2017-01886 was held on December 11, 2018, and a copy of the transcript was entered into the record. Paper 34 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the record before us, RPX has shown, by a preponderance of the evidence, that claims 1–9, 11, 13, and 14 of the '012 patent are unpatentable. RPX, however, has not shown, by a preponderance of the evidence, that claim 10 of the '012 patent is unpatentable.

A. Related Matters

The '012 patent is involved in a district court case titled *IYM Technologies LLC v. Advanced Micro Devices, Inc.*, 1-16-cv-00649-GMS (D. Del) (the "Delaware Litigation"). Pet. vii; Paper 4, 1. In addition to this Petition, RPX filed a separate petition in Case IPR2017-01886 requesting an *inter partes* review of claims 1–14 of the '012 patent. *Id.* A Final Written

Decision for Case IPR2017-01886 is being entered concurrently.

B. The '012 Patent

The '012 patent, titled "Methods and System for Improving Integrated Circuit Layout," issued November 4, 2008, from U.S. Patent Application No. 10/907,814, filed on April 15, 2005. Ex. 1001, [54], [45], [21], [22]. The '012 patent claims priority to the following provisional applications: (1) U.S. Provisional Application No. 60/603,758, filed on August 23, 2004; and (2) U.S. Provisional Application No. 60/564,082, filed on April 21, 2004. *Id.* at [60].

The '012 patent generally relates to integrated circuit ("IC") manufacturing and, in particular, to a method and system for generating and optimizing the layout artwork of an IC. Ex. 1001, 1:11–13. As background, the '012 patent discloses that, in modern processing technology, the manufacturing yield of ICs (i.e., a measure of functioning devices in semiconductor testing) depends heavily on their layout construction. *Id.* at 1:17–19. For a given manufacturing process, a set of design rules are applied during chip layout in order to avoid geometry patterns that cause chip failures. *Id.* at 1:19–21. These design rules guarantee the yield by limiting layout geometry parameters, such as minimum spacing, minimal line width, etc. *Id.* at 1:21–23. Conventional layout construction systems cover the worst case scenario for all chips by applying these design rules over a wide chip area and to entire classes of circuits. *Id.* at 1:24–27.

The '012 patent discloses that, in modern processing technology, many layout features may interact during chip processing. Ex. 1001, 1:29–31. These feature-dependent interactions are difficult to capture with precise design rules and, as a result, sufficiently relaxed global design rules are implemented in order to guarantee the yield. *Id.* at 1:33–36. According to the '012 patent, there are two drawbacks to this approach: (1) it clearly wastes chip area; and (2) determining the worst case scenario in all chips is a non-trivial task that consumes engineering resources. *Id.* at 1:37–40. The '012 patent further discloses that some emerging processing technologies prefer one spatial direction over another. *Id.* at 1:41–42. Existing layout generation systems, however, use identical minimal spacing and minimal width rules for both directions that lead to wasted chip area and underutilization of processing capabilities because the design rules must cover the worst case scenario in both directions. *Id.* at 1:42–46.

The '012 patent purportedly addresses these and other problems by providing a method and system for forming layout constraints to account for local and orientation processing dependencies. Ex. 1001, 1:51–54. By combining a local process modification value, which represents an additional safeguard beyond an original design rule constraint, with the original design rule constraint itself, it effectively creates a new constraint for every unique local situation. *Id.* at 1:55–64, 4:3–5. This mechanism adds extra safeguards to design rule formulation and improves chip yield by eliminating processing hotspots. *Id.* at 1:64–67, 4:5–6.

C. Illustrative Claim

Of the challenged claims, claim 1 is independent and it is directed to a method for generating design layout artwork implemented in a computer. Claims 2–11, 13, and 14 directly depend from independent claim 1. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

1. A method for generating design layout artwork implemented in a computer, comprising:

receiving a design layout comprising a plurality of layout objects residing on a plurality of layers;

receiving descriptions of manufacturing process;

constructing a system of initial constraints among said layout objects;

computing local process modifications to change said initial constraints using said descriptions of manufacturing process;

constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints;

enforcing said new local constraint distances; and

updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances;

whereby a new layout is produced that has increased yield and performance.

Ex. 1001, 8:16–34 (emphasis added).

D. Instituted Grounds of Unpatentability

We instituted trial on the following grounds (Dec. on Inst. 31).

Reference(s)	Basis	Challenged Claim(s)
Allan (Ex. 1015)	§ 103(a)	1–5, 10, 11, 13, and 14

Allan (Ex. 1015) and Kroyan (Ex. 1006)	§ 103(a)	4 and 6–9

II. ANALYSIS

A. Claim Construction

In an *inter partes* review proceeding, claim terms of an unexpired patent are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2017).[4] Under the broadest reasonable interpretation standard, claim terms are generally given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art, in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In its Petition, RPX proposes constructions for the following claim terms: (1) "width," "space," "overlap," enclosure," and "extension" (claim 13); and (2) "description(s) of manufacturing process" (all challenged claims). Pet. 16–18. There is no dispute between the parties regarding the proper construction of these terms.

RPX does not propose a construction for the claim term "constraints," but nonetheless advocates for

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[4] A different rule applies for petitions filed on or after November 13, 2018. Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b)).

a construction of this claim term that is the same as the construction applied by IYM in the Delaware Litigation. Pet. 33–35. According to RPX, in the Delaware Litigation, IYM argued for a broad construction of "constraints" to mean "limits on geometry parameters of the layout objects in the design layout." *Id.* at 33 (citing Ex. 1017, 4). RPX argues that, because the claim construction standard at the Board is broader than the standard applied in district court, IYM should not be allowed to seek a narrower construction of this term in attempting to distinguish Allan. *Id.* at 33–34 (citing *Rembrandt Wireless Techs., LP v. Samsung Elecs. Co.*, Ltd., 853 F.3d 1370, 1377 (Fed. Cir. 2017) ("[T]he Board in IPR [*inter partes* review] proceedings operates under a broader claim construction standard than the federal courts.")). In its Response, IYM does not dispute RPX's proposed construction for the term "constraints." PO Resp. 14–17. After reviewing the record developed during trial, we agree with the parties that an appropriate construction of the term "constraints" is "limits on geometry parameters of the layout objects in the design layout."

The parties, however, dispute the construction of the claim 1 phrase "enforcing said new local constraint distances." PO Resp. 28–36; Pet. Reply 4–8; PO Sur-Reply 1–3. Although RPX does not propose a construction of this phrase in its Petition or Reply, it contends IYM's proposed construction is incorrect. *See* Pet. 15–18; Pet. Reply 4–8.

IYM contends the phrase "enforcing said new local constraint distances" means "finding solutions (i.e., adjustments to the layout) that remove violations of the new local constraint distances," and refers to the claims, Specification, Dr. Nagel's and Dr. Bernstein's cross-examination testimony, and their Declarations as supporting this construction. PO Resp. 17–20 (citing Ex. 1001, 8:26–27, 8:29–32, 4:17–21, 3:65–66, 4:17–54; Ex. 2012 ¶¶ 51–54). IYM also refers to the Delaware Litigation claim interpretation urged by IYM, a dictionary definition, and the "solution" in the next step of claim 1 as supporting this construction. *Id.* at 20–21 (citing Ex. 1017, 13–14; Ex. 2016, 17, 19; Ex. 2017, 472; Ex 2012 ¶ 56).

According to IYM, the Specification describes two embodiments, one of which applies a formula, the other applies heuristic techniques, and each includes removing violations. *Id.* at 17–19 (citing Ex. 1001, 4:25–27, 4:47–49, 8:29–32; Ex. 2012 ¶ 54). IYM then refers to a dictionary definition of "enforcing" as to "compel compliance with (a law, rule, or obligation)," and contends "no reasonable interpretation of the claimed 'enforcing said new local constraint distances' limitations would permit violation of the new local constraint distances to remain without even attempting to fix them." *Id.* at 20 (citing Ex. 2017, 472; Ex. 2012 ¶ 56).

IYM contends this proposed construction is the same construction asserted by IYM in the Delaware Litigation. *Id.* at 20–21 (citing Ex. 1017, 13–14). IYM contends Dr. Nagel's cross-examination testimony contradicts RPX's proposed construction and expressly agrees that the claimed enforcing step "is a step of removing violations of the new local constraint distances," *id.* at 19–20 (citing Ex. 2013, 85:12–86:7; Ex. 2012 ¶ 55):

> Q. … Now, when you enforce the new local constraint distances, isn't it fair to say that the result of that enforcing is a set of new coordinates for the layout objects?

> A. Yes.
>
> Q. Okay. And that set of new coordinates is such that there are no violations of the new local constraint distances d_new?
>
> MR. JOHANNES: Objection. Form.
>
> THE WITNESS: That's correct.
>
> BY MR. PACELLI:
>
> Q. So the enforcing step in Claim 1 of the '012 patent is a step of removing violations of the new local constraint distances; correct?
>
> MR. JOHANNES: Objection. Form.
>
> THE WITNESS: Yes. That's correct.
>
> BY MR. PACELLI:
>
> Q. So after the enforcing step, there should be no violations of the new local constraint distances?
>
> A. That's correct.

Ex. 2013, 85:12–86:7.

IYM also refers to Dr. Bernstein's Declaration, in which he stated "I agree with Dr. Nagel's assessment that the claimed enforcing step 'is a step of removing violations of the new local constraint distances.'" Ex 2012 ¶ 55.

RPX counters that IYM's proposed construction is incorrect. Pet. Reply 4–9. According to RPX, the claim does not recite removing violations and, although the Specification describes two embodiments in which enforcing includes removing violations, these are simply preferred embodiments, and the Specification expressly states the invention is not limited to the disclosed embodiments. *Id.* at 5–8 (citing Ex. 1001, 2:1–4, 2:64–67, 4:17–21, 4:55–67). RPX argues that, even in the preferred embodiment that utilizes a formula, local constraint distances can be enforced even if the original layout does not violate them. *Id.* at 6–7 (citing Ex. 1001, 4:22–44, Fig. 2). According to RPX, "[g]iven that the resulting solution seeks to ensure compliance with all new local constraint distances when making modifications to the original layout, the optimization process seeks to 'enforce' both the 'some of the local constraint distances' that are 'likely' violated and those other local constraint distances that are not violated by the original layout." *Id.* at 7 (citing Ex. 1001, 4:19–42).

RPX refers to the Delaware Litigation in which the U.S. District Court for the District of Delaware ("Court") rejected IYM's current claim construction and commented that it was "puzzling." *Id.* at 4 (citing Ex. 2015, 4 n.4). The Court determined the construction of the phrase is "solving a set of equations after incorporating the new local constraint distances." *Id.* Neither party proposes this construction in this proceeding. When asked about this construction at the oral hearing, RPX's counsel stated the construction would be acceptable, except for inclusion of the term "equation" because the enforcement of inequalities may create uncertainty with respect to "equation." Tr. 38:2–23. According to RPX's counsel, "[i]f you just substitute constraints for equations in the District Court construction, we're fine with that construction." *Id.* at 38:21–23.

RPX characterizes the cross-examination testimony of Dr. Nagel as not supporting IYM's argument that the disputed limitation requires removing violations. Pet. Reply at 9. According to RPX, "Dr. Nagel acknowledged . . . there '***should*** be no violations of the new local constraint distances' that survive the enforcement step. But, importantly, Dr. Nagel was *not asked* if this was 'required' for enforcement of the local constraints, *nor* whether the [broadest reasonable interpretation] of the enforcing step was limited to removing violations." *Id.*

During the oral hearing, RPX's counsel directed us to the cross-examination testimony of Dr. Bernstein. Tr. 34:4–35:3, 107:4–21. The relevant portion of Dr. Bernstein's cross-examination testimony is reproduced below.

> Q. Okay. So just so I'm clear, in the context of the '012 patent, every time step F is performed, violations are removed?
>
> . . .
>
> A. If there are violations, obviously, you have to qualify that, because there may not be a violation depending on the design. We don't know. You could enforce without having a violation.

Ex. 1027, 185:6–13.

We begin our analysis by examining the intrinsic evidence, which supports a claim construction that removal of violations is not required. Upon reviewing the Specification of the '012 patent, we do not find an explicit definition for the phrase "enforcing said new local constraint distances." We, therefore, refer to its ordinary and customary meaning, as would be understood by one of ordinary skill in the art, in the context of the entire disclosure. *Translogic*, 504 F.3d at 1257.

The Specification refers to local constraint enforcement together with removing violations on two occasions. First, when discussing the local constraint enforcement illustrated in Figure 2, the Specification discloses constructing an objective function at block 100, which, "[i]n a preferred embodiment," is used "together with the linear constraint system [to] remove[] the new violations introduced by local constraint with minimal perturbation." Ex. 1001, 4:22–27. When discussing "another preferred embodiment," the Specification discloses that "the violations to local constraints are removed one at a time using heuristic procedures." *Id.* at 4:47–49. Based on these disclosures, we agree with RPX the Specification describes removing violations in the context of preferred embodiments that are exemplary rather than required.

The plain language of independent claim 1 also supports treating the removal of violations as preferred embodiments that are exemplary rather than required. Independent claim 1 recites, in relevant part, "enforcing said new local constraint distances" and "updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances." Ex. 1001, 8:29–32. Notably absent from this claim language is an explicit requirement that enforcement includes removing violations. Instead, this claim language clearly indicates that "solutions" are "obtained from enforcing said new local constraint distances." Obtaining solutions in this context is consistent with both the description of Figure 2 in the Specification and the Court's construction of "solving the set of linear equations after incorporating the new local constraint distances." Ex. 1001, 4:18–54, Fig. 2; Ex. 2015, 4 n.4.

Turning to the extrinsic evidence, the testimony of Drs. Nagel and Bernstein is inconclusive. On the one hand, Dr. Nagel's cross-examination testimony suggests removal of violations is required. Ex. 2013, 85:12–86:7.

On the other hand, Dr. Bernstein's cross-examination testimony suggests removal of violations is not required. Ex. 1027, 185:6–13. On their face, the referenced cross-examination testimony of Drs. Nagel and Bernstein is contrary to the position of their respective party. In addition, we note RPX's counsel's statement at the oral hearing that Dr. Nagel's answer, when viewed in context, does not identify that the broadest reasonable interpretation of the "enforcing" limitation of claim 1 includes removing violations. Tr. 30:19–31:15. We also note RPX's counsel's statement at the oral hearing that Dr. Bernstein's Declaration and cross-examination testimony do not identify that the broadest reasonable interpretation includes removing violations. Tr. 107:4–21 (citing Ex. 1027, 185:6–13, 186:15–22,).

The extrinsic evidence, in the form of the dictionary definition proffered by IYM, also is inconclusive. The CONCISE OXFORD ENGLISH DICTIONARY (11th ed. 2004) defines "enforce" as to "compel compliance with (a law, rule, or obligation)." Ex. 2017, 472. This definition, however, does not account for the scenario where there may not be a violation in the IC design. As Dr. Bernstein testified, "you can enforce without having a violation." Ex. 1027, 185:12–13. As one example, a police officer enforcing a motor vehicle speed limit is not necessarily required to remove violators (e.g., by issuing speeding tickets), particularly when no motor vehicles are exceeding the speed limit. *See* Tr. 115:7–19.

In summary, upon weighing all the evidence bearing on the construction of "enforcing said new local constraint distances," the extrinsic evidence is inconclusive and does not overcome the intrinsic evidence. We agree with RPX that the phrase "enforcing said new local constraint distances" does not require removing violations because the Specification only describes removing violations in the context of preferred embodiments. Instead, we construe this phrase to mean "solving a set of linear equations or constraints after incorporating the new local constraint distances," which is consistent with the description of Figure 2 in the Specification of the '012 patent, the plain language of independent claim 1, and the construction in the Delaware Litigation. Ex. 1001, 4:18–54, 8:29–32, Fig. 12; Ex. 2015, 4 n.4.

B. Obviousness Over the Teachings of Allan

RPX asserts that claims 1–5, 10, 11, 13, and 14 of the '012 patent are unpatentable under § 103(a) over the teachings of Allan. Pet. 27–57. RPX explains how Allan teaches or suggests the subject matter of each challenged claim to one of ordinary skill in the art. *Id.* RPX also relies upon the Declaration of Dr. Nagel to support its positions. Ex. 1002 ¶¶ 101–133, 312–414. In its Response, IYM presents a number of arguments, most of which focus on whether Allan teaches or suggests "enforcing said new local constraint distances," as recited in independent claim 1. PO Resp. 28–38. IYM relies on the Declaration of Dr. Bernstein to support its positions. Ex. 2012 ¶¶ 118–130.

We begin our analysis with the principles of law that generally apply to a ground based on obviousness, followed by an assessment of the level of skill in the art, a brief overview of Allan, and the parties' contentions with respect to the challenged claims.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).[5] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")); see *In re Warsaw Orthopedic, Inc.*, 832 F.3d 1327, 1333 (Fed. Cir. 2016) (citing *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1360 (Fed. Cir. 2006)).

To prevail on its challenges, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is

[5] The parties do not address secondary considerations, which, accordingly, do not form part of our analysis.

unpatentable." *Harmonic Inc. v. Avid Tech., Inc.* 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC. v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner does not satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

2. Level of Skill in the Art

There is evidence in the record before us that enables us to determine the knowledge level of a person of ordinary skill in the art. Relying on the testimony of its declarant, Dr. Nagel, RPX asserts that a person of ordinary skill in the art as of April 2004, which is the earliest priority date on the face of the '012 patent, would be an individual who possesses "a bachelor's degree in Electrical Engineering or the equivalent, along with at least two years of experience in developing and/or researching integrated circuit technology." Pet. 15 (citing Ex. 1002 ¶¶ 30–32). IYM's declarant, Dr. Bernstein, generally agrees with the assessment of RPX and Dr. Nagel, but further clarifies that "a person of ordinary skill in the art would have had a sufficient familiarity with [electronic design automation] tools to be able to competently use such tools and understand their operation." PO Resp. 12–13 (citing Ex. 1002 ¶ 31; Ex. 2012 ¶¶ 26–29).

We do not discern a material difference between the assessments advanced by the declarants, nor does either party premise its arguments exclusively on its assessment of the level of skill in the art. Moreover, each party's declarant appears to meet or exceed both parties' assessments (see Ex. 1002 ¶¶ 2–13; Ex. 1003; Ex. 2012 ¶¶ 3–19, Curriculum Vitae), and either assessment of the level of skill in the art is consistent with the '012 patent and the asserted prior art. We, therefore, adopt Dr. Nagel's assessment and apply it to our obviousness evaluation below, but note that our conclusions would remain the same under Dr. Bernstein's assessment.

3. Allan Overview

Allan "introduces the concept of local design rules" for IC layout optimization at the local level to increase yield. Ex. 1015, 1355. Allan explains that IC layouts are "bound by a set of design rules" that "determine the minimum size and spacing of all layers of the circuit geometry in an attempt to maximize the yield, performance, and reliability." *Id.* Allan explains "the design rules are applied over the whole of the layout area" and are referred to as "global design rules (GDRs)." *Id.* Allan recognizes that these GDRs may give a "good layout . . . but are not necessarily optimized for the local layout conditions." *Id.*

Allan's solution to the non-optimal layout provided by "global" rules is a set of modifications to the global rules, specific to "local layout conditions," which Allan refers to as "local design rules" (LDRs). *Id.* In Figure 1, reproduced below, Allan illustrates an example of its process for increased track widths where permitted by local and global design rules.

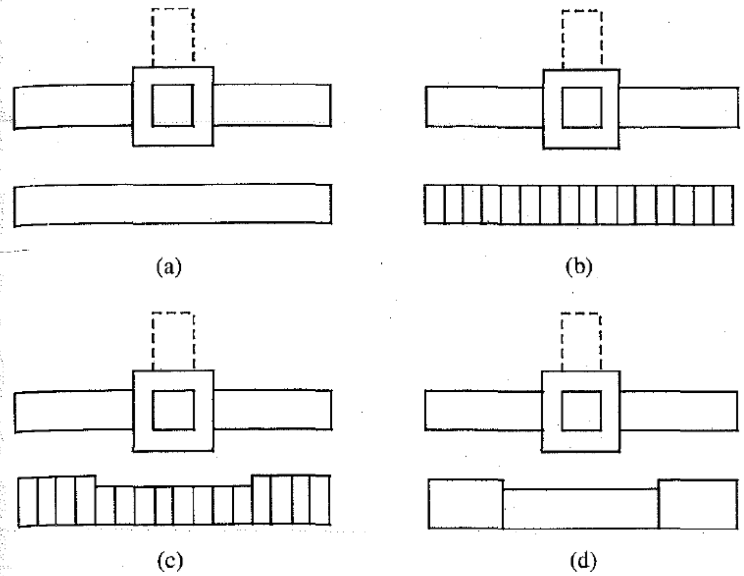

Fig. 1. Application of track width LDR. (a) Original layout. (b) Split track into segments. (c) Increase segment widths where LDR's permit. (d) Merging of segments.

Id. at 1357.

Figure 1(a), reproduced above, describes an "example layout" in which "the bottom metal track has a track width LDR applied to it." *Id.* In Figure 1(b), "the track [width] is split into segments . . . and each segment is tested." *Id.* "If there is space above or below the segment greater than that required for the GDR and the LDR separation, a new wider segment is generated." *Id.* "All the design rules for the new larger segment are checked, and if there are no violations[,] the change in width is accepted," as shown in Figure 1(c). *Id.* In Figure 1(d), the segments are merged. *Id.*

In Figure 2, reproduced below, Allan describes the algorithm used in Figures 1(a)–1(d).

```
Procedure WidthLDR Track
    begin
      Split Track into Segments (see fig. 1(b)).
      for all Segments do {
        if ( Space Above Segment >= LDR + GDR) AND
          ( DesignRuleCheck = OK ) then Increase Segment Size (Top).
        if ( Space Below Segment >= LDR + GDR) AND
          ( DesignRuleCheck = OK ) then Increase Segment Size (Bottom).
      }
      Merge Segments (see fig. 1(d)).
    end
```

Fig. 2. Algorithm for track width LDR.

Id. at 1357.

Figure 2, reproduced above, describes the algorithm used in Figures 1(a)–1(d) wherein the track is split into segments, and for all the segments, if the space above and below the segment is determined to be greater than LDR + GDR, then the segment size can be increased if the design rule check is OK. Then, the segments are merged.

4. Claim 1

RPX contends Allan teaches all the steps recited in independent claim 1. Pet. 27–47 (citing Ex. 1015; Ex. 1002 ¶¶ 312–378). Following institution of trial, IYM argues Allan does not teach the limitation "enforcing said new local constraints" ("disputed limitation") and does not address separately the remaining claim 1 limitations. *See* PO Resp. 28 n.8 ("While Patent Owner believes that Allan is directed to entirely different subject matter from the claimed invention of the '012 Patent, and fails to disclose numerous claim limitations, for ease of explanation Patent Owner focuses solely on the dispositive issue of Allan's failure to disclose the '012

Patent's enforcement of new local constraint distances."). For completeness, in our discussion below, where applicable, we incorporate our analysis of all the claim 1 limitations set forth in the Decision to Institute, and we address the RPX and IYM arguments regarding the disputed limitation.

Beginning with the preamble "[a] method for generating design layout artwork implemented in a computer," RPX contends Allan describes a computer program ("LocDes") that implements Allan's techniques for analyzing and generating a new layout in which the program acts as a postprocessor of Caltech Intermediate Format (CIF) layout, and "uses the GDR layout to produce an enhanced circuit layout[.]" Pet. 28 (citing Ex. 1002, ¶¶ 313–314[6]; Ex. 1015, 1355:§ I, 1356:§ IV). RPX additionally contends Allan's program takes the original layout in CIF format and processes it, using a set of LDRs. *Id.* RPX argues Allan's Figure 9 also shows the program's user interface, which allows the user to apply LDRs to individually selected pieces of circuit geometry. *Id.* (citing Ex. 1015, 1359:§ IV(C)(3), Fig. 9; Ex. 1002 ¶ 314).

RPX contends Allan teaches the step "receiving a design layout comprising a plurality of layout objects residing on a plurality of layers." Pet. 29–31 (citing Ex. 1002 ¶¶ 315–320). RPX argues Allan's CIF layout specification identifies each of the layout's geometric objects, including their coordinates and on what IC layer

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[6] Although RPX cites Exhibit 1002 ¶¶ 313–144, based on the context, we understand Petitioner's citation to be to Exhibit 1002 ¶¶ 313–314.

each object resides. *Id.* at 29 (citing Ex. 1002 ¶ 316; Ex. 1011, 115–27). According to RPX, a person of ordinary skill in the art ("POSA") "would have understood receiving a layout in CIF format would encompass receipt of a layout including multiple objects on multiple layers." *Id.* (citing Ex. 1002 ¶ 316); *see also* Ex. 1015, 1358–59:§ IV(B).

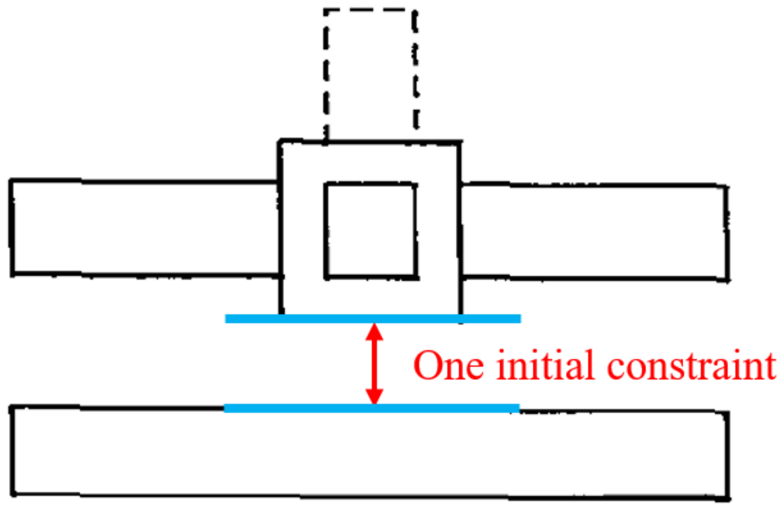
RPX contends that Allan teaches the step "receiving descriptions of manufacturing process." Pet. 16–18, 31–33 (citing Ex. 1002 ¶¶ 321–28). According to RPX, this term should be assigned its plain and ordinary meaning, and a POSA would have understood the plain meaning of "descriptions of manufacturing process" to be consistent with its later use in claim 1—i.e., "computing local process modifications to change said initial constraints using said descriptions of manufacturing process." *Id.* at 16–17. RPX argues a POSA would have understood that the term encompasses sufficient information to enable "computing local process modifications." *Id.*

RPX contends Allan describes receiving design rules and simulation models. *Id.* at 31 (citing Ex. 1002 ¶ 323). RPX further contends a POSA would have understood Allan's "design rules" and "simulation models" to be examples of information describing a "manufacturing process," and this term ("manufacturing process") would be construed to cover one or both of those, and/or other information. *Id.* at 31.

RPX contends defining Allan's GDRs requires knowledge of the process and normally includes the generation of test structures or simulating such test structures. *Id.* at 31 (citing Ex. 1015, 1356:§§ II–II(A)). According to RPX, a POSA would have understood Allan's design rules to be reflective of a manufacturing process. *Id.* at 32 (citing Ex. 1002 ¶ 324). RPX argues Allan notes that deriving LDRs requires even more knowledge of the manufacturing process than GDRs "since the problem is no longer a 'simple' matter of finding one rule set to maximize yield of regular test structures." *Id.* (citing Ex. 1015, 1357:§ II).

RPX argues Allan teaches the step "constructing a system of initial constraints among said layout objects." Pet. 33–37 (citing Ex. 1002 ¶¶ 329–340). RPX argues the application of design rules (and circuit design considerations) during the design process can determine the "constraints" between adjacent layout objects. *Id.* at 34. RPX further argues "[c]onstructing the system of initial constraints," under IYM's construction in the Delaware Litigation, is determining the constraints among layout objects in the design. *Id.* (citing Ex. 1015, 3:16–43; Ex. 1017, 4; Ex. 1002 ¶ 331).

RPX contends Allan describes generating a system of constraints arising from application of the GDRs during the design process, which constrains positioning or other dimensions among layout objects. *Id.* at 35. RPX contends Allan describes a set of GDRs, and producing a layout that has been determined to be compliant with the GDRs. *Id.* (citing Ex. 1015, 1356: § IV(A)) (disclosing that "the original layout has been passed by a design rule checker"). RPX argues determining whether the original layout is compliant with the design rules involves applying the rules to the layout and creating constraints for each layout object. *Id.* According to RPX, for example, Allan's Figure 1 illustrates the result of applying a minimum interobject distance rule between adjacent layout objects, generating a compliant layout. *Id.* Figure 1(a) below, annotated in red and blue by RPX, includes at least two layout objects, which for ease of description can be termed the "top" object and the "bottom" object. *Id.* at 35–36 (citing Ex. 1002 ¶¶ 333–334).



(a)

In annotated Figure 1(a) above, RPX contends the initial constraint of this example is derived from a GDR regulating an interobject distance, wherein the rule may generally specify that two objects may not be closer than some specified minimum distance. *Id.* at 36. RPX additionally contends the rule becomes a constraint on the two objects shown in Figure 1(a)—i.e., the bottom object must be separated from the top object by at least the minimum distance. *Id.* RPX contends the constraint imposed on the bottom object may be expressed as "Space Above Object >= GDR," where "GDR" is the value of the minimum interobject distance specified by the GDR. Annotated Figure 1(a) above shows the initial constraint in red and the edges of the two objects driving the positioning of the two objects according to the constraint in blue. *Id.* (citing Ex. 1002 ¶ 334).

RPX argues because Allan's LocDes program is "a design rule checker" that accepts "only those changes that do not violate any of the global or other local design rules," Allan constructs a "system of initial constraints" (under IYM's construction) that captures the constraints between layout objects in the received design layout. *Id.* at 36–37 (citing Ex. 1015, 1356:§ IV, Ex. 100 ¶¶ 335–336). RPX further argues determining this set of initial constraints between layout objects is "constructing a system of initial constraints among said layout objects." *Id.* at 37 (citing Ex. 1002 ¶ 337).

RPX argues Allan teaches the step "computing local process modifications to change said initial constraints using said descriptions of manufacturing process." Pet. 38–40 (Ex. 1002 ¶¶ 341–349). According to RPX, the '012 patent describes that "local process modification to the design rule constraint distance transforms the global design rule constraints into location specific constraints." *Id.* at 38 (citing Ex. 1001, 3:44–46). RPX contends the '012 patent describes that the "computing" includes either performing simulations to derive the modifications or retrieving a predetermined value from a look-up table. *Id.* (citing Ex. 1001, 5:1–6:2; *see also* Ex. 1001, claims 8 and 9; Ex. 1002 ¶¶ 342–343).

RPX argues the values specified by Allan's LDRs are the "local process modifications." *Id.* at 38. According to RPX, Allan describes techniques to compute the values for the LDRs, which may be stored for use by its program, and Allan also explains that the values of the LDRs are "changes" to the initial constraints. *Id.* (citing Ex. 1015, 1355–56:§ II; Ex. 1002 ¶ 343).

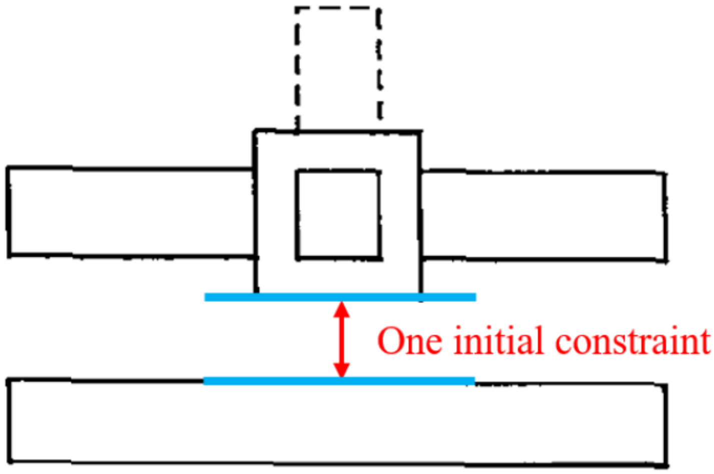
RPX contends Allan describes evaluating a layout using LDRs "to determine where changes in layout generated from GDR set[s] should be performed." *Id.* (citing Ex. 1015, 1355:§ II). RPX further argues Allan's LDRs are the "local process modifications," as recited in claim 1. *Id.* RPX argues the LDRs define variations in object dimensions with respect to the original GDRs, based on local conditions within an IC layout. *Id.* According to RPX, Allan specifically observes that "[t]here are a number of potential layout changes that can be made as follows: track displacement, increased contact size . . . , increased contact overlap, increased track width." *Id.* at 38–39 (citing Ex. 1015, 1355:§ I). According to RPX, Allan's LDRs, which are the local process modifications, change the initial constraints (specifying values derived from the global rules) on a layout. *Id.* at 39 (citing Ex. 1002 ¶ 344).

RPX contends Allan's design rules, including its local design rules, are generated using information on a manufacturing process that is to be used, and are reflective of that manufacturing process. *Id.* (citing Ex. 1015, 1355:§ II.). RPX contends LDRs are applied to GDR-generated layouts to achieve this further local optimization. *Id.* RPX additionally contends Allan also discloses that, "[w]hile it is intended that the yield of the resulting layout will be greater than the initial GDR layout, *this can be guaranteed only if the fabrication process is understood well enough* to ensure that the LDRs are an accurate reflection of the relative yield of the layout options under test." *Id.* (citing Ex. 1015, 1355:§ I).

RPX contends the Allan LDRs are computed using the received simulation models. *Id.* at 40. RPX contends the GDRs and the simulation models are a "description of manufacturing processes." *Id.* RPX contends Allan explains that multiple LDRs can be derived from the simulation results. *Id.* (citing Ex. 1015, 1356:§ II(A)). According to RPX, a POSA would have appreciated that, when a tool "applies" an LDR in this manner, the LDR would be predefined, based on the simulations as discussed above, and that the "value" for the LDR would be retrieved from storage. *Id.* (citing Ex. 1002 ¶ 347). RPX contends retrieving the value for an LDR from a data storage falls within the scope of "computing" a local process modification in this limitation. *Id.* (citing Ex. 1002 ¶ 348).

RPX argues Allan teaches the step "constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints." Pet. 40–43 (citing Ex. 1002 ¶¶ 350–361). According to RPX, Allan discloses constructing new local constraint distances by creating new constraints for existing and/or new layout objects, and by combining values specified by LDRs (the local process modifications) with the constraint distances in the initial constraints. *Id.* at 40 (citing Ex. 1002 ¶ 351).

RPX argues Allan describes an example of "constructing new local constraint distances." *Id.* at 41. Allan's Figure 1(a), below, annotated by RPX, shows the initial constraint.



(a)

Figure 1(a) annotated by RPX to show one initial constraint

RPX argues Allan's Figure 1(b), below, annotated by RPX, illustrates that an original object, to which the single initial constraint was applied, is divided into a set of local objects, such that a local constraint may be identified as a modification of the single initial constraint. *Id.*

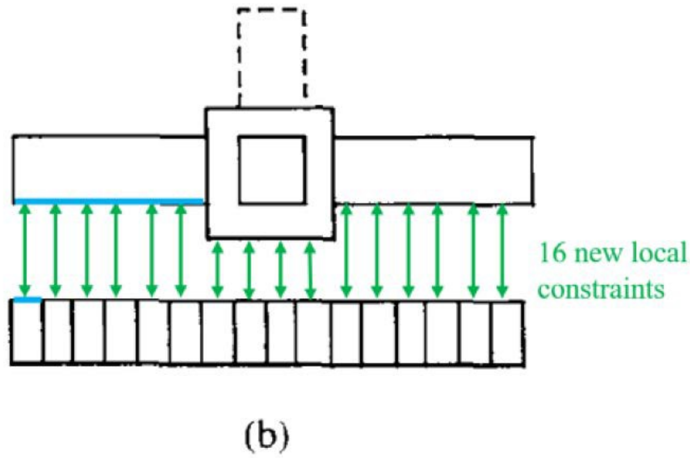


Figure 1(b) annotated by RPX to show 16 new local constraints.

RPX argues the new local constraint distances include a constraint distance for each of the new bottom objects (with the existing, top object), where before there was a single constraint, and the new local constraint distances also result from modifying the initial constraint to have a different constraint distance. *Id.* at 41–42. RPX also argues Allan describes that a local value for an LDR is added to an initial value from the initial constraint (the GDR) to yield the value for the new local constraint. *Id.* at 42. According to RPX, the new local constraints may even be evaluated using different edges in the layout, as illustrated by comparing the blue lines in annotated Figure 1(b) above. *Id.* (citing Ex. 1002 ¶¶ 352–355).

RPX argues Allan's process leverages the new constraint distances to determine whether and how it can make adjustments to the layout, wherein the new local constraints are evaluated for each local layout object and constrain the ability of Allan's process to make adjustments to the layout in the area of that local layout object. *Id.* (citing Ex. 1015, 1356:§§ I, IV (disclosing that the process "attempts small changes in layout based on the LDR's," accepts "only those changes that do not violate any of the global or other local design rules," and "no changes are made to the layout except where there is good evidence to suggest that a higher yield can be obtained") Ex. 1002 ¶ 356)).

RPX argues, in Figure 2, annotated by RPX below, Allan illustrates the new local constraint for each local object, and the process of constructing a new local constraint distance by combining a local process modification with a constraint distance for an initial constraint (*id.*):

if (Space Above Segment >= $LDR + GDR$) **AND**

(DesignRuleCheck = OK) **then** Increase Segment Size (Top).

RPX argues, in annotated Figure 2 above, the constraint for each of the multiple "bottom" objects are "Space Above Segment >= LDR + GDR," and the new local constraint is created by combining a local process modification value (specified by an LDR) with the constraint distance specified by the initial constraint (specified by a GDR). *Id.* at 43. RPX argues this new local constraint differs from the initial constraint discussed above regarding Figure 1(a): "Space Above Object >= GDR". *Id.* (citing Ex. 1002 ¶¶ 357–358).

RPX argues each combination of LDR + GDR (i.e., each new local constraint distance) constrains a modification that could be made by Allan's LocDes program. *Id.* According to RPX, in Allan's Figure 2, the combination LDR + GDR constrains whether and how much the track width can be increased by a distance between objects, and therefore creates a "new local constraint distance." *Id.* (citing Ex. 1015, 1357:§ IV(A)(1) ("If there is space above or below the segment greater than that required for the GDR and the LDR separation, a new wider segment is generated. All the design rules for the new larger segment are checked, and if there are no violations, the change in width is accepted (Fig. l(c))."); Ex. 1002 ¶ 359).

In view of the above, we determine that RPX has met its burden to show, by a preponderance of the evidence, that Allan teaches or suggests the above limitations of claim 1.

The disputed limitation: "enforcing said new local constraint distances"

As discussed in our claim construction section, *supra*, RPX and IYM dispute the construction of the phrase "enforcing said new local constraint distances" wherein RPX contends this phrase does not require removing violations and IYM contends this phrase requires removing violations. We agree with RPX's construction that this phrase does not require removing violations because the Specification only describes removing violations in the context of preferred embodiments. Instead, we construe this phrase to mean "solving a set of equations or constraints after incorporating the new local constraints," which is consistent with the description of Figure 2 in the Specification of the '012 patent, the plain language of independent claim 1, and the construction in the Delaware Litigation. Ex. 1001, 4:18–54, 8:29–32, Fig. 12; Ex. 2015, 4 n.4.

RPX argues Allan teaches the disputed limitation as properly interpreted. Pet. 43–44; Pet. Reply 3–10. Alternatively, RPX argues that, even applying IYM's alleged incorrect and narrow interpretation requiring removing violations, Allan still teaches the disputed limitation. Pet. Reply 10–19. We begin our analysis by addressing RPX's position that Allan teaches the disputed limitation as properly interpreted and then we turn to RPX's alternative position.

RPX argues Allan teaches the step "enforcing said new local constraint distances." Pet. 43–44 (citing Ex. 1002 ¶¶ 362–365). RPX argues Allan evaluates opportunities for modifying the layout geometry in accordance with the local design rules, so long as such modifications do not violate any of the constraints. *Id.* (citing Ex. 1015, 1356:§ IV (LocDes program "accept[s] only those changes that do not violate any of the global or other local design rules.").

RPX argues Allan discloses that the algorithm in Figure 2 is "used by the program to *adjust layout*." *Id.* at 44 (citing Ex. 1015, 1356:§ IV(A), Fig. 2 (showing that the conditional "if (Space Above/Below Segment >= LDR + GDR)" enforces the new constraint by permitting movement up until this condition fails)). RPX argues the "DesignRuleCheck" in combination with "Space Above/Below Segment >= LDR + GDR" enforces the constraints. *Id.* (citing Ex. 1002 ¶ 364).

In its Response, IYM contends Allan does not teach removing violations and, therefore, does not teach or suggest the disputed limitation. PO Resp. 28–33. According to IYM:

> In summary, in Allan, either (i) a track segment's width is increased because there are no violations of the purported "new local constraint distances" (i.e., "LDR+GDR"), or (ii) a track segment's width is not increased precisely because the layout violates (and continues to

> remain in violation of) the purported new local constraint distances. In either situation, Allan plainly does not teach the claimed step of "enforcing said new local constraint distances," and in fact it teaches quite the opposite: if there is a violation, leave it; if there is none, keep increasing the track segment until a violation is created. Ex. 2012, Bernstein Dec. at ¶ 123.

Id. at 33.

In its Reply, RPX argues Allan discloses the disputed limitation because the claim does not require removing violations, and notes "IYM had every opportunity to draft the claims more narrowly to be limited to removing violations of new local constraint distances but did not." Pet. Reply 4–9.

In its Sur-Reply, IYM argues its proposed claim construction (requires removing violations) applies and argues, "[i]f, however, the claimed method is able to successfully remove at least some existing violations, then 'enforcement' has occurred." PO Sur-Reply 1–2 (citing Ex. 1027, 218:5–221:12; 341:5–342:10).

Based on the record developed during trial, we agree with RPX because, under the correct construction (removing violations is not required), Allan teaches the disputed limitation. In particular, as discussed, *supra*, Space Above/Below Segment >=LDR+GDR are constraints that are enforced in Allan because the modifications to the layout resulting from LDR+GDR solve problems arising from an initial set of GDRs without violating any other GDRs or LDRs. Ex. 1015, 1356. Stated differently, after incorporating the new local constraints (i.e., LDRs) into the GDR constraints, Allan solves the initial problems arising from these GDRs by permitting movement without violating any other GDRs or LDRs. We credit Dr. Nagle's testimony, referring to Figure 2 of Allan, that the conditional "if (Space Above/Below Segment >= LDR + GDR) enforces the new constraint by permitting movement up until this condition fails" because this testimony is consistent with the teachings in Allan discussed above. Ex. 1002 ¶ 364.

Additionally, assuming *arguendo* that the disputed limitation requires removing violations, RPX argues Allan also teaches the disputed limitation. Pet. Reply 11. According to RPX, Allan's "Increase Track Width" enforces new local constraint distances and is done by "imposing new local **maximum** constraint distances on the **available space** above and below each new segment." *Id.* (citing Pet. 22–27; Ex. 1015, Figs. 1, 2, 1355–57). According to RPX, the LocDes program decreases the space above/below until the space above/below is no longer greater than or equal to the new maximum local constraint distance ("LDR + GDR"), at which point no further increases in the segment size will be made. *Id.* at 13. RPX then argues "the routine thus seeks to remove violations of the new local maximum constraint on the space above/below the segment by increasing the segment until the maximum constraint on the free space above/below the segment is no longer violated–i.e., the space above/below is less than LDR+GDR." *Id.* at 13–14 (citing Allan at 1355–57).

In its Sur-Reply, IYM argues RPX's argument in its Reply that Allan's LDR+GDR is a maximum constraint on the space between tracks should not be entitled to consideration because it is a new argument that should have been raised earlier. Sur-Reply 3 (citing *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369–70 (Fed. Cir. 2016)). According to IYM, RPX's position is inconsistent with the position taken in the Petition that the space above segments must be greater than, or equal to, "'LDR+GDR'--an alleged minimum spacing requirement." *Id.* at 3–4. IYM further argues RPX's assertion of a maximum constraint is not supported by the record and notes there is no Reply declaration from Dr. Nagel supporting this position and, therefore, no citation to Dr. Nagel's testimony. *Id.* at 5–6. According to IYM, Allan limits track increase to 1.5x the minimum track width, 1.5x the minimum spacing, no global design rules are violated, and includes no requirement to keep increasing track width until the space falls below LDR+GDR. *Id.* at 6–8 (citing Ex. 1015 at 1360, Ex. 1027, 238:18–240:13, 146:6–147:12).

We agree that RPX's argument that Allan's LDR+GDR is a *maximum* constraint on the space between tracks is a new argument presented for the first time in the Reply Brief. Although a constraint may be a minimum or a maximum constraint, based on the record developed during trial, RPX's belated presentation of this argument unfairly prejudices IYM and, therefore, should not be entitled to consideration.

Remaining undisputed claim 1 limitations

RPX argues Allan teaches the step "updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances." Pet. 44–45 (citing Ex. 1002 ¶¶ 366–371). RPX contends Allan describes that its program "produce[s] an enhanced circuit layout" and "adjust[s] layout" by using LDRs "to determine where changes in layout … should be performed." *Id.* at 44 (citing Ex. 1015, 1355:§§ I–II, 1356:§ IV(A)). RPX argues, as shown in Figure 2 of Allan and discussed *supra*, if the "if" statement is satisfied, then track width is increased. *Id.* at 45. According to RPX, if these conditions are satisfied, the layout geometry is modified, and then stored in a data structure. *Id.* (citing Ex. 1015, 1358–59:§ IV(B), Fig. 2); *see also* Ex. 1015, Fig. 1, 1357:§ IV(A)(1); Ex. 1002 ¶¶ 368–370.

Finally, RPX argues to the extent that the "whereby" clause in claim 1 is limiting, Allan discloses "whereby a new layout is produced that has increased yield and performance." Pet. 45–47 (citing Ex. 1002 ¶¶ 372–376). RPX argues that in the Delaware Litigation, IYM contends that the phrase "whereby a new layout is produced that has increased yield and performance" is part of a "whereby" clause "that is not limiting and therefore does not need to be construed." *Id.* at 46 (citing Ex. 1017, 15). RPX argues IYM should not be permitted to take a contrary, narrower position here. *Id.* (citing *Rembrandt*, 853 F.3d at 1377 ("[T]he Board in IPR proceedings operates under a broader claim construction standard than the federal courts.").

RPX argues Allan is titled "An Yield Improvement Technique for IC Layout Using Local Design Rules," which describes that design rules are used to constrain IC layouts "*in an attempt to maximize the yield, performance*, and reliability." *Id.* (citing Ex. 1015, 1355:§ I). RPX contends Allan discloses that "*[t]he yield can be increased* by more effective use of silicon area through the application of local design rules to layouts that have been generated from the normal 'global' design rules." *Id.* (citing Ex. 1015, 1362:§ VI ("Local design rules can be used to *increase the yield* in processes that suffer from conductor shorts, contact problems, and conductor breaks[.]")). According to RPX, a POSA would have understood that Allan's techniques are intended to generate a new layout resulting in fabricated integrated circuits with increased yield and performance. *Id.* (citing Ex. 1002 ¶¶ 374–375).

In view of the above, we determine that RPX has met its burden to show, by a preponderance of the evidence, that Allan teaches or suggests the remaining undisputed limitations of claim 1.

Other claim 1 issues

IYM argues (1) Allan addresses a fundamentally different problem than the one addressed by the '012 patent because Allan doesn't disclose the same solution provided by the '012 patent; and (2) RPX blurs the line between anticipation and obviousness. Prelim. Resp. 23–42.

Regarding the fundamentally different problem, IYM contends the '012 Patent is directed to solving a hotspot problem not addressed by Allan, whereas Allan is directed to a very different problem of the best use of any redundant space on an initial layout. *Id.* at 23–24.

Based on the record developed during trial, we are not persuaded by IYM's argument in this regard because claim 1 does not recite hotspots, much less solving a hotspot problem. Ex. 1001, 8:16–34. We note dependent claim 6 recites hotspots (*id.* at 8:48–53); however, RPX's challenge to claim 6 is not based on Allan alone, but instead is based on Allan in combination with Kroyan. Pet. 67–68. In addition, we note that it is well-settled that simply because a reference has a different objective does not preclude a person of ordinary skill in the art from using its teachings in an obviousness evaluation. *See In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) ("The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. . . ."); *see also EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985) ("A reference must be considered for everything that it teaches, not simply the described invention or a preferred embodiment.").

We also are not persuaded by IYM's argument that RPX blurs the line between anticipation and obviousness. Prelim. Resp. 25–26. Regarding obviousness based on Allan alone, RPX explains:

> The claims call out specific features that do not contribute to the purported inventiveness of the '012 patent and are instead the type of information that publications in this field typically assume is within the reader's knowledge and do not explicitly discuss. For this reason, . . . obviousness grounds are presented rather than anticipation, even where a single reference is cited. Dr. Nagel's testimony is cited for these well-known features, together with supporting evidence.

Pet. 8.

Under the circumstances described by RPX, it is appropriate to apply a single prior art reference—in this case, Allan—together with the background knowledge of one of ordinary skill in the art—as evidenced by Dr. Nagel's supporting testimony—in analyzing obviousness. *See Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1346–47 (Fed. Cir. 2018) ("Though less common, in appropriate circumstances, a patent can be obvious in light of a single prior art reference if it would have been obvious to modify the reference to arrive at the [claimed] invention.") (quoting *Arendi S.A.R.L. v. Apple Inc.*, 832

F.3d 1355, 1361 (Fed. Cir. 2016)); *see also Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (affirming the Board's conclusion that claims were obvious based on one prior art reference alone, notwithstanding patent owner's argument that the ground at issue would have been more properly raised under 35 U.S.C. § 102).

Summary

In view of the above, we find RPX has shown, by a preponderance of the evidence, that the subject matter of claim 1 is unpatentable over Allan.

5. Dependent claims 2–5, 13, and 14

RPX contends Allan teaches the limitations of dependent claims 2–5, 13, and 14. Pet. 47–57 (citing Ex. 1015; Ex. 1002 ¶¶ 379–398, 406–414). IYM does not address separately RPX's explanations and supporting evidence as to how the teachings of Allan account for the limitations of dependent claims 2–5, 13, and 14. *See generally* PO Resp. 24–47. We have reviewed RPX's explanations and supporting evidence regarding these dependent claims, and we agree with and adopt RPX's analysis showing that the teachings of Allan account for all the limitations recited in dependent claims 2–5, 13, and 14. *See* Pet. 47–57. RPX, therefore, has shown, by a preponderance of the evidence, that dependent claims 2–5, 13, and 14 are unpatentable over Allan.

6. Claim 10

Regarding claim 10, RPX argues Allan discloses "the step of enforcing new local constraint distances comprises optimizing a predefined objective function for optimizing measurable performance of a layout, subject to said new local constraint distances." Pet. 53 (citing Ex. 1002 ¶¶ 398–401). According to RPX, in its enforcement of new local constraint distances, Allan discloses "optimizing a predefined objective function." *Id.* RPX contends, in the pseudocode (Figure 2), Allan discloses predefined objective functions—namely, that distances meet certain LDR + GDR statements—without violating "any of the global or other local design rules." *Id.* (citing Ex. 1015, 1356:§ IV; Ex. 102l ¶¶ 399–400).

RPX contends Allan explains that the initial GDRs "are not necessarily optimized for the local layout conditions." *Id.* (citing Ex. 1015, 1355:§I). According to RPX, Allan's LDRs "define the *best values* of track width and contact size/overlap in relation to the local layout conditions" and RPX contends Allan notes "that the yield of circuits fabricated-using layout generated from a GDR set can be increased by searching for instances of local nonoptimal layout, applying an LDR set, and adjusting the layout to meet the new design rules." *Id.* According to RPX, this optimization is done in accordance with LDRs, which are design rules that "attempt to maximize . . . performance." *Id.* at 54 (citing Ex. 1015, 1355:§I ("[Design] rules determine the minimum size and spacing of all layers of the circuit geometry in an attempt to maximize the yield, performance, and reliability."); Ex. 1002 ¶ 401).

IYM contends Allan does not disclose the limitation of dependent claim 10. PO Resp. 38–42. According to IYM, referring to a dictionary definition, an objective function is "the function of which one seeks the optimum [e.g., maximum or minimum] in an optimization problem, especially one with constraints." *Id.* at 39 (citing Ex. 2021 at 396, 401 (Collins Dictionary of Mathematics (2d ed. 2002))). IYM argues, "Consistent with that definition, the '012 patent describes an embodiment for enforcing the new local constraint distances through the use of 'an objective function Ct*X, where Ct is a row vector of coefficients for achieving various optimization objectives.'" *Id.* (citing Ex 1001 at 4:22–24). According to IYM, in this embodiment, the enforcing step solves the linear system of minimizing Ct*X, subject to the new local constraint distances. *Id.* (citing Ex. 1001, 4:35–36; Ex. 2012 ¶ 133).

Applying this definition, IYM argues Allan simply discloses three algorithms for attempting to take advantage of unused layout space and RPX appears to rely on the "if" statements discussed, *supra*, that allow a layout object to be moved on the conditions that there is sufficient space and no design rules will be violated. *Id.* at 40 (citing Pet. 53). According to IYM, the "if" statement "cannot be an "objective function" because Allan does not attempt to minimize or maximize it. *Id.* IYM argues Dr. Nagel's statement that Allan's "Increase Segment Size (Top)" is an instruction to increase segment size, not an objective function to be optimized. *Id.* at 40 (citing Ex. 1002 ¶ 400; Ex. 2012 ¶ 134). IYM further argues RPX's characterization of Allan is incorrect and based on partial and out of context quotations. *Id.* For example, according to IYM, Allan's reference to "best values" is merely laudatory and RPX's contention that Allan's optimization is done in accordance with LDRs that attempt to maximize performance is incorrect because Allan is referring to global design rules, not local design rules. *Id.* at 41–42 (citing Pet. 53–54; Ex. 1015, 1355, 1356; Ex. 2012 ¶ 135).

In its Reply Brief, RPX, once again, refers to Allan's LocDes Program and Dr. Nagel's explanation that Allan discloses predetermined objective functions—namely, that distances meet certain LDR+GDR statements—without violating any of the global or other local design rules. Pet. Reply 19 (citing Pet. 53–54; Ex. 1002 ¶¶ 398–401). According to RPX, Allan's LocDes Program seeks to locally optimize the width of every track segment by minimizing the free space above/below the segment by optimizing the objective function and thereby maximize the width of the track segment to increase yield. *Id.* at 20 (citing Ex. 1015, § II A. 2–3). RPX notes Allan's statement, "[w]hile this will not necessarily give the optimal layout, it will produce a good approximation to it in a reasonable time." *Id.* at 21 (citing Ex. 1015, 1356: § IV). RPX then argues "an objective function is one that seek the optimum" and that is what Allan does by optimizing the layout pursuant to the imposed constraints. *Id.*

In its Sur-Reply, IYM submits that RPX presents an impermissible first time argument–that Allan seeks to maximize the track width by minimizing available spaces above/below it–because the Petition only alleged that "Allan discloses predetermined objective functions, namely that distances meet certain LDR+GDR statements." PO Sur-Reply 9 (citing Pet. 53; Pet. Reply 20). IYM also further argues Allan does not seek to minimize the space between tracks, because any decrease in spacing is subject to conditions on track width increase. *Id.*

Based on the record developed during trial, we are not persuaded by RPX's arguments, particularly because, although Allan teaches, subject to the constraints, minimizing the free space above/below the segment by optimizing the objective function and *increasing* the width of the track segment to increase yield, RPX specifically argues Allan teaches *maximizing* the width of the track segment. We agree with IYM that this is an impermissible new argument. Petitioner's arguments prior to the Reply Brief address only the minimum constraints >= LDR + GDR and they do not characterize the constraint as seeking to maximize the track width by minimizing available spaces above/below it. *Compare* Pet. 53–54, *with* Pet. Reply 20. This argument appears for the first time in the Reply Brief and appears to be directed to IYM's uncontested proffered definition, *supra*, that an "objective function is the function of which one seeks the optimum (e.g., maximum or minimum) in an optimization problem, especially one with constraints." Additionally, RPX's arguments regarding claim 10 are not persuasive because RPX has not demonstrated sufficiently that the width is maximized.

In view of the above, we find RPX has not shown, by a preponderance of the evidence, that the subject matter of claim 10 is unpatentable over Allan.

7. Claim 11

RPX contends claim 11 is written in Markush format, as it recites the phrase "selected from a group consisting of." Pet. 54 (citing *Abbott Labs. v. Baxter Pharm. Prod., Inc.*, 334 F.3d 1274, 1280 (Fed. Cir. 2003)). As such, RPX contends Allan need only disclose one of the three listed objective functions to disclose this limitation and Allan discloses at least two of the limitations of claim 11. *Id.* (citing Nagel ¶¶ 402–405).

Regarding the first limitation, "objective function for legalizing the layout with minimal changes from the original layout," RPX argues Allan states that "no changes are made to the layout except where there is good evidence to suggest that a higher yield can be obtained." *Id.* (citing Allan, 1355:§ I). RPX argues Allan further cautions "that any changes that result from the application of LDRs to a layout do not cause a degradation in performance of the circuit." *Id.* (citing Allan, 1356:§ III). According to RPX, Allan's procedure thus "legaliz[es] the layout" (with respect to the LDRs) "with minimal changes from the original layout" (by virtue of not making unnecessary or harmful changes). *Id.* at 54–55 (citing Nagel ¶ 404).

In its Response, IYM argues Allan's changes are not "minimal" as Allan makes many changes, including unnecessary changes. PO Resp. 42–44 (citing Pet. 54–55; Allan Figs. 12 (a), (b)); Ex. 1015, 1361; Ex. 2013; Tr. 127:9–16, 124:7–24; 126:12–14; Ex. 2012 ¶ 138). IYM argues Allan teaches its methods are used only "once the area has been defined," and does not attempt to optimize the layout at all." *Id.* at 46 (citing Ex. 1015 at 1355; Ex. 2013, 157:2–17, 123:18–25, 152:24–153:2; Ex. 2012 ¶¶ 140, 141).

In its Reply Brief, RPX counters that Allan's objective function (Space Above/Below Segment>= LDR+GDR), discussed *supra*, establishes that no change is made based on LDRs unless good evidence exists that it would increase yield and not degrade performance. Pet. Reply 21 (citing Pet. 54–55). According to RPX, like the '012 patent, Allan makes changes only because they are believed to increase yield. *Id.* at 22 (citing PO Resp. 42; Ex. 1002 ¶ 42; Ex. 2012 ¶ 37; Ex. 1001, Abstract, 3:1–3; Tr. 5:22–6:5, 65:18–20).

IYM asserts in its Sur-Reply that RPX reiterates in its Reply that Allan does not change a layout "unless 'good evidence' exists that it would increase yield and not degrade performance," while ignoring Patent Owner's evidence that Allan's techniques do not "legaliz[e] the layout with minimal changes." PO Sur-Reply 9 (citing Reply Br. at 21). According to IYM, RPX's' unsupported argument that Allan's undefined "good evidence" results in minimal layout changes is contradicted by Allan's teachings and Dr. Nagel's testimony. *Id.* (citing Resp. at 42–43).

Based on the record developed during trial, we are persuaded by RPX's arguments, particularly Allan's teaching that "no changes are made to the layout except where there is good evidence to suggest that a higher yield can be obtained." Ex. 1015, 1355, § I. Allan expressly teaches no changes are made, except where there is good evidence to suggest higher yield, and IYM's assertions to the contrary, regarding purported unnecessary changes, do not outweigh the express general teaching of Allan. Thus, we are persuaded that Allan teaches the claim 11 limitation "objective function for legalizing the layout with minimal changes from the original layout."

Therefore, we find RPX has shown, by a preponderance of the evidence, that Allan teaches this limitation. Because claim 11 is written in Markush format, RPX has shown Allan teaches the subject matter of this claim by teaching one of the three limitations recited therein. *See supra.*

C. Obviousness Over the Combined Teachings of Allan and Kroyan

RPX contends that claims 4 and 6–9 of the '012 patent are unpatentable under § 103(a) over the combined teachings of Allan and Kroyan. Pet. 64–71. RPX explains how this proffered combination teaches or suggests the subject matter of each challenged claim, and provides reasoning as to why one of ordinary skill in the art would have been prompted to modify the references' teachings. *Id.* RPX also relies upon the Declaration of Dr. Nagel to support its positions. Ex.

1002 ¶¶ 416–61. IYM's arguments solely focus on dependent claim 9. PO Resp. 47–52. IYM relies on the Declaration of Dr. Bernstein to support its positions. Ex. 2012 ¶¶ 142–147.

We begin our analysis with a brief overview of Kroyan, and then we address the parties' arguments and evidence with respect to dependent claim 9.

1. Kroyan Overview

Kroyan generally relates to a system and method for designing ICs fabricated by a semiconductor manufacturing process and, in particular, to designing ICs to enhance manufacturability and improve yield. Ex. 1006, 1:22–28. Figure 3 of Kroyan, reproduced below, illustrates a method for IC design in accordance with one embodiment. *Id.* at 4:43–45.

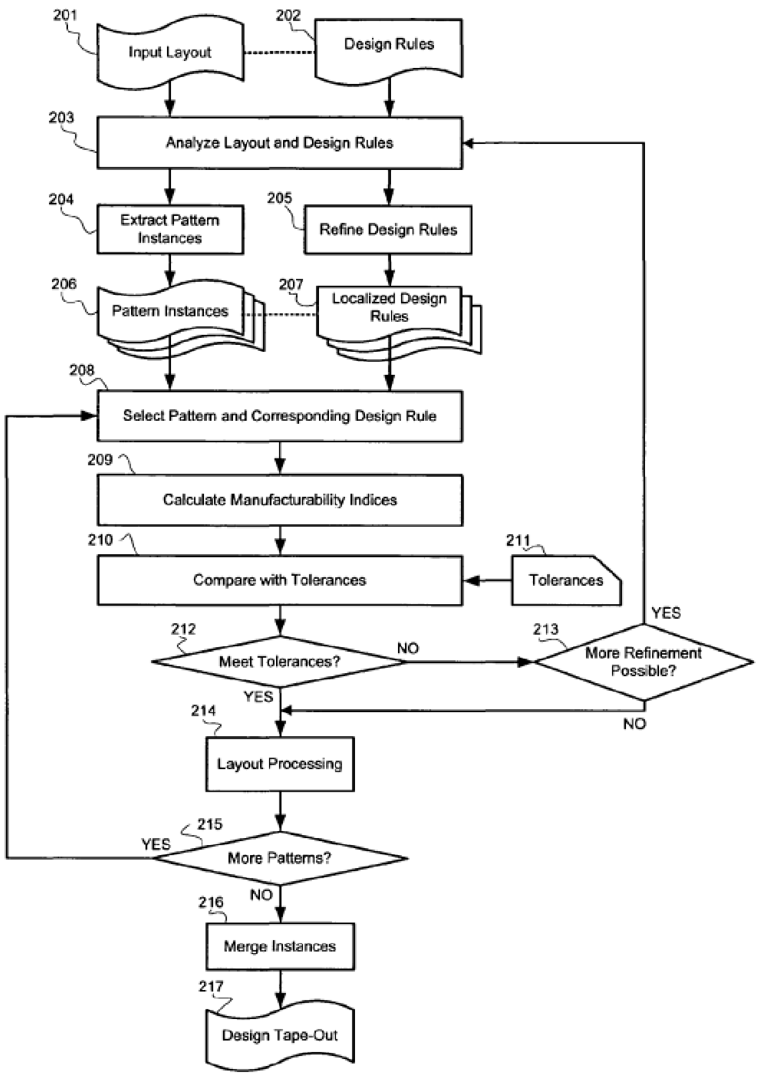


Figure 3

Figure 3 of Kroyan, reproduced above, illustrates that, at step 203 the analysis engine receives input layout 201 and design rules 202. *Id.* at 5:63–66. The analysis engine evaluates the layout and design rules by determining distinct pattern types that "have different criticality leading to different manufacturability margin requirements." *Id.* at 6:4–7. In step 204, certain pattern instances 206 are extracted. *Id.* at 6:17–18. Similarly, at step 205, localized design rules are produced that correspond to each extracted pattern instance. *Id.* at 6:18–20. At step 208, each pattern instance and localized design rule is selected for an evaluation of manufacturability indices at step 209. *Id.* at 6:20–23. At step 210, the results of calculating the manufacturability indices are compared against past tolerances 211. *Id.* at 6:30–31. In step 212, if the results are within the tolerances, the selected design rules are suitable for the given pattern instances. *Id.* at 6:31–34. The process then proceeds to step 214, where the layout is processed according to these selected design rules. *Id.* at 6:34–35. At step 213, if more refinement is needed, the process returns to step 203 for further analysis. *Id.* at 6:35–39.

Figure 9 of Kroyan, reproduced below, illustrates a flow diagram of an intelligent analysis and optimization resolution enhancement technique in accordance with another embodiment. Ex. 1006, 4:62–64.

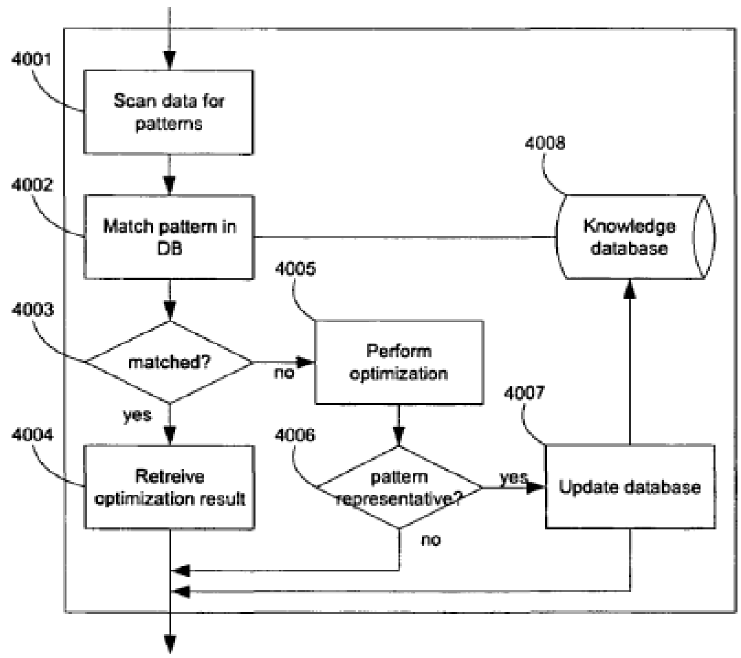


Figure 9

Figure 9 of Kroyan, reproduced above, illustrates that, at step 4001, the input design layout first is scanned and, at step 4002, the output layout patterns are compared against data stored in database 4008. *Id.* at 9:1–5. At step 4003, if a match is found, an optimization result is retrieved at step 4004. *Id.* at 9:6–7. At step 4005, if a match is not found, then a decision is made whether to store the results in the database at step 4006. *Id.* at 9:7–11. If the results are stored, database 4008 is updated at step 4007. *Id.* at 9:11–12.

2. Claims 4 and 6–8

IYM does not address separately RPX's explanations and supporting evidence as to how the teachings of Allan and Kroyan account for the limitations of dependent claims 4 and 6–8. *See generally* PO Resp. 47–52. We have reviewed RPX's explanations and supporting evidence regarding these dependent claims, and we agree with and adopt RPX's analysis showing that the combined teachings of Allan and Kroyan account for all the limitations recited in dependent claims 4 and 6–8. *See* Pet. 64–71. RPX, therefore, has shown, by a preponderance of the evidence, that the subject matter of dependent claims 4 and 6–8 is unpatentable over Allan and Kroyan.

3. Claim 9

Claim 9 depends from independent claim 1, and further recites "wherein the step of computing local process modification comprises searching a look-up data table." Ex. 1001, 8:63–65.

In its Petition, RPX contends that the '012 patent states that a "local process modification value" for adjusting a layout constraint can be determined from either simulation or using "look-up data tables" that store "pattern recognition." Pet. 71 (citing. Ex. 1001, 5:1–6:2; Ex. 1002 ¶ 456). RPX argues that Kroyan's knowledge database may be used to retrieve an "associated remedial solution" that could be provided to an optimizer. *Id.* (citing Ex. 1006, 9:1–7, 10:46–58, 11:55–12:3). According to RPX, Kroyan's "associated remedial solution" that is provided to the optimizer constitutes the "local process modification," recited in independent claim 1. *Id.* (citing Ex. 1002 ¶¶ 457–460). In the Allan and Kroyan combination, RPX argues that Kroyan's knowledge database would be used to identify a value for an LDR to be applied and, therefore, teaches the limitation of dependent claim 9. *Id.* (citing Ex. 1002 ¶ 461).

Turning to the rationale to combine the teachings of Allan and Kroyan, RPX contends that it would have been obvious to a person of ordinary skill in the art to generate a knowledge database, as taught by Kroyan, to facilitate the analysis of the layout and GDRs, and eventual application of the LDRs, as taught by Allan. Pet. 61 (citing Ex. 1002 ¶ 421). According to RPX, developing a knowledge database is a simple design choice for using a particular data structure that achieves the predictable result of being able to "best capture known problematic patterns and apply the appropriate treatment." *Id.* (quoting Ex. 1006, 8:6–8) (citing Ex. 1002 ¶ 421)).

In its Response, IYM argues a person of ordinary skill in the art would have no motivation to combine the teachings of Kroyan with those of Allan to result in the limitation of dependent claim 9. PO Resp. 47–52. In particular, IYM argues a POSA would have no motivation to combine Kroyan's purported "lookup data table" with Allan's local design rules. *Id.* at 47 (citing Ex. 2012 ¶ 142). According to IYM, Dr.'s Nagel's statement that a POSA would know how to make the combination is insufficient, as it does not indicate why a POSA would be motivated to make the combination. *Id.* at 48–49 (citing Ex. 1002 ¶¶ 461, 421; Ex. 2012 ¶ 143; Pet. 60–61; *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068–69 (Fed. Cir. 2018) (improper to "focus[] on what a skilled artisan would have been able to do, rather than what a skilled artisan would have been motivated to do at the time of the invention")). IYM argues RPX's reliance on a "simple design choice" is conclusory. *Id.* at 49 (citing Ex. 1006 8:6–8; Ex. 1002 ¶ 421; Pet. 61).

According to IYM, Allan discloses three LDRs and there would be no reason to resort to Kroyan's knowledge database, which includes a large amount of data storing a comprehensive set of problematic patterns and associated remedial solutions. *Id.* at 49–51 (citing Ex. 1006 11:66–12:2; Ex. 2013, 170:12–15, 170:17–20, 172:1–2, 172: 9–21, 172:22–173:6; Ex. 2012 ¶ 144). IYM argues Kroyan's knowledge database serves a purpose not relevant to Allan, as Kroyan needs a database of storing and quickly accessing a "comprehensive set" of unique "problematic patterns" and their associated remedial solutions." *Id.* at 50–51 (citing Ex. 1006, 11:65–12:2; Ex. 2013 172:1–7; Ex. 2012 ¶ 145). IYM argues that Dr. Nagel agreed that Allan's three LDRs apply to all metal tracks in the layout and, therefore, a POSA would not look to Kroyan's knowledge database to select an LDR based on wire and contact geometry patterns, "because the same LDRs would apply to *every* geometry pattern." *Id.* at 51–52 (citing Ex. 2013, 173:23–175:12; Pet. 60; Ex. 2012 ¶¶ 146, 147).

In its Reply Brief, RPX argues that Allan searches for instances of local non-optimal layout and applies LDRs to adjust the layout, and a POSA would have reason to use a lookup table like Kroyan's (which includes images of non-optimal layouts and solutions to them) to identify non-optimal portions of Allan's layout and to provide LDRs to address these non-optimal layouts, because doing so simply applies Kroyan's known technique for achieving these results, and it would have been an obvious design choice to implement in Allan. Pet. Reply 24 (citing Pet. 59–64). According to RPX, developing a knowledge database is a simple design choice for using a particular data structure that achieves the predictable result of being able to "*best capture* known problematic patterns and apply the appropriate treatments." *Id.* at 25 (quoting Ex. 1006, 8:6–8) (citing Pet. 60–61; Ex. 1002 ¶ 421). RPX additionally argues the lookup table would store a different value to assign to the LDR for different non-optimal configurations. *Id.*, citing Pet. at 59–64. RPX argues IYM's assertion that Allan uses only three LDRs is wrong as Dr. Nagel testified that there are "three types of LDR's," not "only three LDR's," and Dr. Nagel testified there would be thousands of LDRs in Allan. *Id.* at 25 (citing PO Resp. 50; Ex. 2013, 172:22–173:6). According to RPX, Allan does not teach that every instance of a type of LDR must share the same value because different values for the same type of LDR (e.g., for increasing track width) may be applied to different areas of the layout, and a lookup table, as taught by Kroyan, was an obvious way to store predefined LDR values for different nonoptimal local layout conditions. *Id.* at 25–26 (citing Pet. 59–64).

In its Sur-Reply, IYM argues RPX did not address IYM's assertion that Allan teaches width LDRs generally apply 1.5x minimum spacing throughout the layout, regardless of the shape and form of the patterns. PO Sur-Reply 10 (citing PO Resp. 51–52; Ex. 1015, 1360). IYM additionally argues that RPX"s new assertion that a "'lookup table would store a *different value* to assign to the LDR for different non[-] optimal configuration' is not present in the Petition and it is not supported by any evidence." *Id.*

Based on the record developed during trial, RPX has shown sufficiently that one of ordinary skill in the art would have combined the teachings of Allan and Kroyan. We credit Dr. Nagle's testimony that Allan and Kroyan each are directed to locally adjusting global constraints to improve yield because this is consistent with their respective disclosures. Ex. 1002 ¶ 418. We also credit Dr. Nagle's testimony that "[a] POSA would have known to generate a knowledge database, as disclosed in Kroyan, in order to facilitate the analysis of the layout and GDRs, and ultimate application of the LDRs, as disclosed in Allan," because "developing a knowledge database is no more than a simple design choice of using a particular data structure that achieves the predictable result of being able to '*best capture* known problematic patterns and apply the appropriate treatment.'" *Id.* at ¶ 421 (citing Ex. 1006, 8:6–8).

As stated by the Supreme Court, an obviousness determination must be based on

> some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

KSR., 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Here, the skilled artisan would "be able to fit the teachings of multiple patents together like pieces of a puzzle" since the skilled artisan is "a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 420–21. Based upon the teachings of Allan and Kroyan identified above, using Kroyan's knowledge database to store Allan's different values assigned to the LDR for different non-optimal configurations is likely to be obvious when it does no more than yield predictable results. *See id.* at 415–16. Moreover, as discussed *supra*, RPX provided persuasive reasons why one of ordinary skill in the art would combine Allan and Kroyan in the manner suggested—namely, to '*best capture* known problematic patterns and apply the appropriate treatment.'" Ex. 1006, 8:6–8 (emphasis added).

In view of the above, we determine Petitioner has shown, by a preponderance of the evidence, that the subject matter of claim 9 is unpatentable over Allan and Kroyan.

D. Constitutional Challenge

IYM contends that the Supreme Court's decision in *Oil States Energy Services, LLC v. Greene's Energy Group, LLC*, 138 S. Ct. 1365 (2018) was limited to addressing *Oil States*'s constitutional challenge that subjecting its patent to an *inter partes* review proceeding violates its right to a jury trial under the Seventh Amendment of the U.S. Constitution. PO Resp. 52–53. IYM noted that that Supreme Court emphasized that its *Oil States* decision "should not be misconstrued as suggesting that patents are not property for purposes of the Due Process Clause or the Takings Clause." *Id.* (quoting *Oil States*, 138 S. Ct. at 1379).

IYM contends that our exercise of jurisdiction to adjudicate the patentability of the '012 patent would violate its rights under the Takings Clause of the Fifth Amendment of the U.S. Constitution, because this patent issued in November 2008, several years prior to the enactment of the America Invents Act ("AIA"). PO Resp. 53. According to IYM, the retroactive nature of this *inter partes* review proceeding underscores the unconstitutionality of the entire process. *Id.* IYM also argues that subjecting the '012 patent to an *inter partes* review proceeding "places a severe, disproportionate, and extremely retroactive burden on" IYM. *Id.* (quoting *E. Enters. v. Apfel*, 524 U.S. 498, 538 (1998)).

RPX counters in its Reply that IYM does not offer any substantive analysis to support its argument that subjecting the ’012 patent to an *inter partes* review proceeding violates IYM’s rights under the Takings Clause. Pet. Reply 26. RPX further contends that IYM does not cite to any authority that would authorize the Board to determine that the “retroactive” application of the AIA is unconstitutional. *Id.*

We decline to consider IYM’s constitutional challenge because “administrative agencies [generally] do not have jurisdiction to decide the constitutionality of congressional enactments.” *See Riggin v. Office of Senate Fair Employment Practices*, 61 F.3d 1563, 1569 (Fed. Cir. 1995); *see also Harjo v. Pro-Football, Inc.*, 50 USPQ2d 1705, 1710 (TTAB 1999) (“[T]he Board has no authority . . . to declare provisions of the Trademark Act unconstitutional.”), *rev’d on other grounds*, 284 F. Supp. 2d 96 (D.D.C. 2003). *But see Am. Express Co. v. Lunenfeld*, Case CBM2014-00050, slip op. at 9–10 (PTAB May 22, 2015) (Paper 51) (“[F]or the reasons articulated in *Patlex* [*Corp. v. Mossinghoff*, 758 F.2d 594 (Fed. Cir. 1985)], we conclude that covered business method patent reviews, like reexamination proceedings, comply with the Seventh Amendment.”).

III. CONCLUSION

We conclude that RPX demonstrates, by a preponderance of the evidence, that (1) claims 1–5, 11, 13, and 14 are unpatentable under 35 U.S.C § 103(a) over Allan and (2) claims 4 and 6–9 are unpatentable under 35 U.S.C § 103(a) over Allan and Kroyan. RPX, however, has not demonstrated by a preponderance of the evidence that claim 10 is unpatentable under 35 U.S.C § 103(a) over Allan.

IV. ORDER

Accordingly, it is

ORDERED that claims 1–9, 11, 13, and 14 of the ’012 patent are held to be unpatentable;

FURTHER ORDERED that it has not been demonstrated that claim 10 of the ’012 patent is unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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APPENDIX E

NOTE: This order is nonprecedential.

United States Court of Appeals for the Federal Circuit

IYM TECHNOLOGIES LLC,
Appellant

v.

RPX CORPORATION, ADVANCED MICRO DEVICES, INC.,
Appellees

2019-1761

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01886.

ON PETITION FOR PANEL REHEARING AND REHEARING EN BANC

Before PROST, *Chief Judge*, NEWMAN, LOURIE, DYK, MOORE, O'MALLEY, REYNA, WALLACH, TARANTO, CHEN, HUGHES, and STOLL, *Circuit Judges*.

PER CURIAM.

O R D E R

Appellant IYM Technologies LLC filed a combined petition for panel rehearing and rehearing en banc. The petition was referred to the panel that heard the appeal, and thereafter the petition for rehearing en banc was referred to the circuit judges who are in regular active service.

Upon consideration thereof,

IT IS ORDERED THAT:

The petition for panel rehearing is denied.

The petition for rehearing en banc is denied.

The mandate of the court will issue on May 15, 2020.

FOR THE COURT

May 8, 2020
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

APPENDIX F

NOTE: This order is nonprecedential.

United States Court of Appeals for the Federal Circuit

IYM TECHNOLOGIES LLC,
Appellant

v.

RPX CORPORATION, ADVANCED MICRO DEVICES, INC.,
Appellees

2019-1762

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017- 01888.

ON PETITION FOR PANEL REHEARING

Before LOURIE, MOORE, and HUGHES, *Circuit Judges*.

PER CURIAM.

O R D E R

Appellant IYM Technologies LLC filed a petition for panel rehearing.

Upon consideration thereof,

IT IS ORDERED THAT:

The petition for panel rehearing is denied.

The mandate of the court will issue on May 15, 2020.

FOR THE COURT

May 8, 2020
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

APPENDIX G

United States Court of Appeals for the Federal Circuit

IYM TECHNOLOGIES LLC,
Appellant

v.

RPX CORPORATION, ADVANCED MICRO DEVICES, INC.,
Appellees

2019-1762

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01888.

JUDGMENT

THIS CAUSE having been considered, it is

ORDERED AND ADJUDGED:

DISMISSED AS MOOT

ENTERED BY ORDER OF THE COURT

March 13, 2020	/s/ Peter R. Marksteiner
Date	Peter R. Marksteiner
	Clerk of Court