APPENDIX A

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED.,
Appellant,
v.
KINGSTON TECHNOLOGY COMPANY, INC.,
Appellee

UNITED STATES,
Intervenor

2018-1768

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2016-01621.

Decided: January 31, 2020

MATTHEW D. POWERS, Tensegrity Law Group LLP, Redwood Shores, CA argued for appellant. Also represented by JENNIFER ROBINSON; AZRA HADZIMEHMEDOVIC, AARON MATTHEW NATHAN, SAMANTHA A. JAMESON, McLean, VA; NATHAN NOBU LOWENSTEIN, KENNETH J. WEATHERWAX, Lowenstein & Weatherwax LLP, LOS ANGELES, CA.

MICHAEL JOHN BALLANCO, Fish & Richardson PC, Washington, DC, argued for appellee. Also represented by DAVID M. HOFFMAN, Austin, TX.

MELISSA N. PATTERSON, Appellate Staff, Civil Division, United States Department of Justice, Washington, DC, argued for intervenor. Also represented by COURTNEY DIXON, DENNIS FAN, SCOTT R. MCINTOSH, JOSEPH H. HUNT; THOMAS W. KRAUSE, JOSEPH MATAL, FARHEENA YASMEEN RASHEED, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA.

Before REYNA. WALLACH, and HUGHES, *Circuit Judges.*

PER CURIAM.

In its opening brief, Polaris Innovations Limited argues that the final written decision at issue in this appeal exceeds the scope of the Patent Trial and Appeal Board's authority and violates the Constitution's Appointments Clause. *See* Appellant's Br. 52 (citing U.S. Const. art. II, § 2, cl. 2). This court recently decided this issue in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019). Accordingly, the Board's decision in No. IPR2016-01621 is vacated, and the case is remanded to the Board for proceedings consistent with this court's decision in *Arthrex.*

VACATED AND REMANDED

COSTS

No costs.

APPENDIX B

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED.,
Appellant,
v.
KINGSTON TECHNOLOGY COMPANY, INC.,
Appellee

UNITED STATES,
Intervenor

2018-1831

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-00116.

Decided: January 31, 2020

MATTHEW D. POWERS, Tensegrity Law Group LLP, Redwood Shores, CA argued for appellant. Also represented by JENNIFER ROBINSON; AZRA HADZIMEHMEDOVIC, AARON MATTHEW NATHAN, SAMANTHA A. JAMESON, McLean, VA; NATHAN NOBU LOWENSTEIN, KENNETH J. WEATHERWAX, Lowenstein & Weatherwax LLP, LOS ANGELES, CA.

DAVID M. HOFFMAN, Fish & Richardson PC, Austin, TX, argued for appellee. Also represented by

MICHAEL JOHN BALLANCO, Washington, DC; NIKITA GUPTA FIORELLA, Wilmington, DE

MELISSA N. PATTERSON, Appellate Staff, Civil Division, United States Department of Justice, Washington, DC, argued for intervenor. Also represented by COURTNEY DIXON, DENNIS FAN, SCOTT R. MCINTOSH, JOSEPH H. HUNT; THOMAS W. KRAUSE, JOSEPH MATAL, FARHEENA YASMEEN RASHEED, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA.

Before REYNA. WALLACH, and HUGHES, *Circuit Judges*.

Opinion for the court filed PER CURIAM.

Concurring opinion filed by *Circuit Judge* HUGHES, in which *Circuit Judge* WALLACH joins.

PER CURIAM.

In its opening brief, Polaris Innovations Limited argues that the final written decision at issue in this appeal exceeds the scope of the Patent Trial and Appeal Board's authority and violates the Constitution's Appointments Clause. *See* Appellant's Br. 52 (citing U.S. Const. art. II, § 2, cl. 2). This court recently decided this issue in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019). Accordingly, the Board's decision in No. IPR2016-01621 is vacated, and the case is remanded to the Board for proceedings consistent with this court's decision in *Arthrex*.

VACATED AND REMANDED

COSTS

No costs.

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED.,
Appellant,
v.
KINGSTON TECHNOLOGY COMPANY, INC.,
Appellee

UNITED STATES,
Intervenor

2018-1831

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-00116.

HUGHES, *Circuit Judge,* concurring, in which WALLACH, *Circuit Judge,* joins.

I concur because we are bound by the prior panel decision in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019).[1] However, I write

[1] The parties have raised the same arguments on the merits of the Appointments Clause issue in both Polaris cases before this panel, Nos. 2018-1768 and 2018-1831. However, the government contends that Polaris waived its Appointments Clause challenge in No. 2018-1768 because it failed to make the argument before the Board in the first instance. I need not address the waiver issue because this concurrence addresses only the merits of the Appointments Clause argument. And I

separately to note that I disagree with the merits and question the remedy of the Arthrex panel decision. I believe that viewed in light of the Director's significant control over the activities of the Patent Trial and Appeal Board and Administrative Patent Judges, APJs are inferior officers already properly appointed by the Secretary of Commerce.

But if APJs are properly considered principal officers, I have grave doubts about the remedy Arthrex applied to fix their unconstitutional appointment. In the face of an unconstitutional statute, our role is to determine whether severance of the unconstitutional portion would be consistent with Congress's intent. Given the federal employment protections APJs and their predecessors have enjoyed for more than three decades, I find no legislative intent to divest APJs of their Title 5 removal protections to cure any alleged constitutional defect. Because the bar to find non-severability is so high, though, I reluctantly agree with Arthrex's remedy.

I

None of the parties here or in *Arthrex* dispute that APJs are officers who exercise "significant authority pursuant to the laws of the United States." *Buckley v. Valeo*, 424 U.S. 1, 126 (1976) (per curiam). But "significant authority" marks the line between an officer and an employee, not a principal and an inferior officer. Despite being presented with the opportunity to do so, the Supreme Court has declined to "set forth an

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address this concurrence to No. 2018-1831 because the parties agree the issue was pre-served there.

exclusive criterion for distinguishing between principal and inferior officers for Appointments Clause purposes." *Edmond v. United States*, 520 U.S. 651, 661 (1997).

Instead, the pertinent cases make clear that the hall-mark of an inferior officer is whether a presidentially-nominated and senate-confirmed principal officer "direct[s] and supervise[s] [her work] at some level." *Id.* at 663. *Edmond* does not lay out a more exacting test than this, and we should not endeavor to create one in its stead. The cases employ an extremely context-specific inquiry, which accounts for the unique systems of direction and supervision in each case. *See infra* Section I. Finally, *Edmond* also makes clear that the Appointments Clause seeks to "pre-serve political accountability relative to important government assignments." 520 U.S. at 663. The current structure for appointing, directing and supervising, and re-moving APJs allows such political accountability through the Director's significant, substantive supervision of APJs' work, and the ability to discipline and terminate APJs to promote the efficiency of the service.

Arthrex, in my view, pays insufficient attention to the significant ways in which the Director directs and super-vises the work of the APJs and, instead, focuses on whether the Director can single-handedly review and reverse Board decisions, and whether APJs are removable at will. In doing so, the *Arthrex* panel essentially distills the Supreme Court's direction and supervision test into two discrete questions: (1) are an officer's decisions reviewable by a principal officer and (2) is the officer removable at will? Be-cause I believe that the Supreme Court

would have announced such a simple test if it were proper, I respectfully disagree with the *Arthrex* panel decision that APJs are principal officers. The Director's power to direct and supervise the Board and individual APJs, along with the fact that APJs are already removable under the efficiency of the service standard, suffices to render APJs inferior officers.

A

The Director may issue binding policy guidance, institute and reconsider institution of an *inter partes* review, select APJs to preside over an instituted *inter partes* review, single-handedly designate or de-designate any final written decision as precedential, and convene a panel of three or more members of his choosing to consider rehearing any Board decision. The *Arthrex* panel categorized some of these as "powers of review" and others as "powers of supervision," but I view them all as significant tools of direction and supervision.

As *Arthrex* recognized, "[t]he Director is 'responsible for providing policy direction and management supervision' for the [United States Patent and Trademark Office]." 941 F.3d at 1331 (quoting 35 U.S.C. § 3(a)(2)(A)). Not only can the Director promulgate regulations governing *inter partes* review procedures, but he may also prospectively issue binding policy guidance "interpreting and applying the pa-tent and trademark laws." Gov't. Br. 21. APJs must apply this guidance in all subsequent *inter partes* review proceedings. Such guidance might encompass, for instance, exemplary application of the law to specific fact patterns, such as those posed in pending cases. These powers provide the Director with control over

the process and substance of Board decisions. Gov't. Br. 8, 21. And though the Director cannot directly reverse an individual Board decision that neglects to follow his guidance, APJs who do so risk discipline or removal under the efficiency of the service standard applicable under Title 5. *See infra* Section I C. Such binding guidance, and the consequences of failing to follow it, are powerful tools for control of an inferior officer.[2]

The Director also has unreviewable authority to institute *inter partes* review. 35 U.S.C. § 314(a), (d). *Cf. Free Enter. Fund v. Pub. Co. Accounting Oversight Bd.*, 561 U.S. 477, 504 (2010) (discussing the importance of the ability to "start, stop, or alter individual [PCAOB] investigations," even where the reviewing principal officer already had significant "power over [PCAOB] activities"). Though the Arthrex panel did not address the Director's ability to reconsider an institution decision, our precedent also holds that the Board[3] may reconsider and reverse its initial institution decision. *See, e.g., Medtronic, Inc. v. Robert Bosch Healthcare Sys., Inc.*, 839 F.3d 1382, 1385–86 (Fed. Cir. 2016) (explaining that "§ 318(a) contemplates that a proceeding can be

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[2] To be sure, I do not mean to suggest that the Direc-tor's extensive powers of supervision mean that he can dic-tate the outcome of a specific inter partes proceeding. Rather, his ability to issue guidance and designate prece-dential opinions provides the general type of supervision and control over APJs' decision-making that renders them inferior, not principal, officers.

[3] The Director's delegation of his institution power to the Board does not diminish its existence. 37 C.F.R. § 42.4(a) (stating that "[t]he Board institutes the trial on behalf of the Director"). *See also Ethicon Endo-Surgery, Inc. v. Covidien LP*, 812 F.3d 1023, 1033 (Fed. Cir. 2016).

'dismissed' after it is instituted, and, as our prior cases have held, administrative agencies possess inherent authority to reconsider their decisions, subject to certain limitations, regardless of whether they possess explicit statutory authority to do so" (internal quotation and citation omitted)).

The Director also controls which APJs will hear any given instituted *inter partes* review. 35 U.S.C. § 6(c). In my view, this power of panel designation is a quintessential method of directing and controlling a subordinate. Importantly, I do not believe that in stating that the power to remove an officer at-will from federal employment is "a powerful tool for control of an inferior," *Free Enterprise*, 561 U.S. at 510 (internal quotation omitted), the Supreme Court meant that such removal power is the only effective form of control in the context of the Appointments Clause. For example, the Judge Advocate General in Edmond could remove the Court of Criminal Appeal judges from judicial service without cause, but not necessarily federal employment altogether. *Edmond*, 520 U.S. at 664. See also *Free Enterprise*, 561 U.S. at 510 (relying on both at-will removal authority and "the [SEC's] other oversight authority" in finding with "no hesitation" that the PCAOB members are inferior officers). That is akin to the Director's authority to designate which APJs will consider a certain case. And despite acknowledging that "when a statute is silent on removal, the power of removal is presumptively incident to the power of appointment[,]" the *Arthrex* panel declined to opine on the Director's ability to de-designate APJs from a panel under § 6(c). *Arthrex*, 941 F.3d at 1332. But *Edmond* referenced the ability to remove the judges

there "from [their] judicial assignment[s]," followed by a recognition of the potent power of removal. 520 U.S. at 664. If the Director's ability to control APJs plays a significant part in the unconstitutionality at issue, such that the remedy is to make APJs removable at will, the panel should have definitively addressed the Director's de-designation authority. Moreover, as outlined in Section I C, *infra*, APJs already may be disciplined or removed from federal employment under the routine efficiency of the service standard, which is not incompatible with discipline or removal for failing to follow the Director's binding guidance.

And the Director may continue to provide substantial direction and supervision after the Board issues its final written decision. As *Arthrex* discusses, the Director may convene a Precedential Opinion Panel (POP), of which the Director is a member, to consider whether to designate a decision as precedential. *Arthrex*, 941 F.3d at 1330. But I read the Standard Operating Procedures more broadly, such that the Director may also make a precedential designation or de-designation decision single-handedly,[4] thereby unilaterally establishing binding

[4] "No decision will be designated or de-designated as precedential or informative without the approval of the Director. This SOP does not limit the authority of the Director to designate or de-designate decisions as precedential or informative, or to convene a Precedential Opinion Panel to review a matter, in his or her sole discretion without regard to the procedures set forth herein." Patent Trial and Ap-peal Board, Standard Operating Procedure 2 (Revision 10) at 1 (Standard Operating Procedure 2), *available at* https://www.uspto.gov/sites/default/files/documents/SOP 2%20R10%20FINAL.pdf.

agency authority on important constitutional questions and other exception-ally important issues. Standard Operating Procedure 2, at 3–4. Indeed, it appears that the Director has done so in at least sixteen cases in 2018 and 2019. *See* USPTO, *Patent Trial and Appeal Board Precedential and informative decisions, available at* https://www.uspto.gov/patents-applica-tion-process/patent-trial-and-appeal-board/precedential-informative-decisions (listing decisions designated as precedential in the past year, where some are labeled as "Precedential Opinion Panel decision" and others are not). The Director may also convene a POP of his choice, of which he is by default a member, to consider whether to rehear and reverse any opinion. Standard Operating Procedure 2, at 4. And, the Director may "determine that a panel of more than three members is appropriate" and then choose those additional members as well. *Id*. Though the *Arthrex* panel recognized these powers, it dismissed them because the Di-rector has only one vote out of at least three. 941 F.3d at 1331–32. This assessment, however, fails to recognize the practical influence the Director wields with the power to hand-pick a panel, particularly when the Director sits on that panel. The Director's ability to unilaterally designate or de-designate a decision as precedential and to convene a POP of the size and composition of his choosing are there-fore important tools for the direction and supervision of the Board even after it issues a final written decision.[5]

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[5] The *Arthrex* panel's underestimation of the Director's power is particularly evident in light of this court's prior en banc decision in *In re Alappat*, 33 F.3d 1526 (Fed. Cir. 1994),

Combined, all of these powers illustrate that the Director has constitutionally significant means of direction and supervision over APJs—making them inferior officers un-der the rule of *Edmond*.

B

Despite the Director's significant powers of direction and supervision, the *Arthrex* panel concluded that APJs are principal officers in large part because no principal officer may "single-handedly review, nullify or reverse" the Board's decisions. *Arthrex*, 941 F.3d at 1329. But Supreme Court precedent does not require such power. And in the cases in which the Court emphasized a principal officer's power of review, that principal officer had less authority to direct and supervise an inferior

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abrogated on other grounds by In re Bilski, 545 F.3d 943 (Fed. Cir. 2008). Alappat contained strong lan-guage about the ability to control the composition and size of panels. *See, e.g., id*. at 1535 (noting that "the Board is merely the highest level of the Examining Corps, and like all other members of the Examining Corps, the Board operates subject to the Commissioner's overall ultimate authority and responsibility"). While the duties of the Board and the Director have changed since *Alappat* was decided, the authority to determine the Board's composition for re-consideration of an examiner's patentability determination mirrors the current authority with respect to *inter partes* review. *Compare* 35 U.S.C. § 6(c) (2012) (giving the Director authority to designate "at least 3 members of the Patent Trial and Appeal Board" to review "[e]ach appeal, derivation proceeding, post-grant review, and *inter partes* review"), *with* 35 U.S.C. § 7(b) (1988) (giving the Commissioner power to designate "at least three members of the Board of Appeals and Interferences" to review "ad-verse decisions of examiners upon applications for pa-tents"). Therefore, I believe the panel should have at least discussed how *Alappat's* view of the power to control the Board might impact the Appointments Clause analysis.

officer's work ex ante than the Director has here.

In *Edmond*, for instance, the Court of Appeals for the Armed Forces, an Article I court, could review decisions of the Court of Criminal Appeals judges at issue. However, its scope of review was limited. *Edmond*, 520 U.S. at 665 (explaining that the Court of Appeals for the Armed Forces may only reevaluate the facts when there is no "competent evidence in the record to establish each element of the offense beyond a reasonable doubt"). And while the Judge Advocate General "exercise[d] administrative oversight" and could "prescribe uniform rules of procedure," he could "not attempt to influence (by threat of removal or other-wise) the outcome of individual proceedings." *Id.* at 664. Nonetheless, the Supreme Court found that the Court of Criminal Appeals judges were inferior, not principal, officers. In comparison, while the Director may not unilaterally decide to rehear or reverse a Board decision, he has many powers to direct and supervise APJs both ex ante and ex post, Section I A, *supra*, that no principal officer had in *Edmond*.

Similarly, in *Freytag v. Comm'r*, 501 U.S. 868 (1991), the Supreme Court considered the status of special trial judges appointed by the Tax Court, whose independent decision-making varied based on the type of case before them. The Court held that the special trial judges were inferior officers—not employees—when presiding over "declaratory judgment proceedings and limited-amount tax cases" be-cause they "render[ed] the decisions of the Tax Court" in those cases. *Id.* at 882. In doing so, the Court distinguished between cases in which the special trial judges acted as "inferior officers who

exercise independent authority," and cases in which they still had significant discretion but less independent authority. *Id.* The Court's analysis distinguished between inferior officer and employee; no-where did the Court suggest that special trial judges' "in-dependent authority" to decide declaratory judgment proceedings and limited-amount cases rendered them principal officers. *See id.* at 881–82. Most recently, the Court applied the framework of *Freytag* in deciding whether administrative law judges (ALJs) of the Securities and Ex-change Commission (SEC) are inferior officers or employees. *Lucia v. S.E.C.*, 138 S. Ct. 2044, 2053 (2018). The Court reasoned that SEC ALJs and *Freytag's* special trial judges are extremely similar, but SEC ALJs arguably wield more power because their decisions become final if the SEC declines review. *Id.* at 2053–54. But again, the Court found this structure still only rendered SEC ALJs officers, not employees. *Id.* at 2054. No mention was made of SEC ALJs being principal officers.[6] *See id.* at 2051 n.3 (explaining that the distinction between principal and inferior officers was "not at issue here"). Just as the special trial judges in *Freytag* and the SEC ALJs in *Lucia* were inferior officers, so too are APJs.

Nor does this court's precedent require unfettered review as a marker of inferior officer

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[6] In fact, the Court declined "to elaborate on *Buckley's* 'significant authority' test" marking the line between officer and employee, citing two parties' briefs which argued that the test between officer and employee, not principal and inferior officer, should include some measure of the finality of decision making. *Lucia*, 138 S. Ct. at 2051–52.

status. In *Masias v. Sec'y of Health & Human Servs.*, we rebuffed the argument that because the Court of Federal Claims does not review decisions of the Vaccine Program's special masters de novo, the special masters are principal officers. 634 F.3d 1283, 1293–94 (Fed. Cir. 2011). There, we recognized that the Court of Federal Claims may only "set aside any findings of fact or conclusions of law of the special master found to be arbitrary, capricious, an abuse of discretion, or other-wise not in accordance with law . . . ." *Id.* at 1294. This limited review means that many of the special masters' decisions are effectively final because the Court of Federal Claims has no basis to set aside findings of fact or conclusions of law. We reasoned that such limited review of special masters' decisions by the Court of Federal Claims resembled the review in *Edmond*, and that "the fact that the review is limited does not mandate that special masters are necessarily 'principal officers.'" *Id.* at 1295.

Finally, the panel analogized the *Arthrex* issue to the one addressed by the D.C. Circuit in *Intercollegiate Broad. Sys., Inc. v. Copyright Royalty Bd.*, 684 F.3d 1332 (D.C. Cir. 2012). *See Arthrex*, 941 F.3d at 1334. But the facts of *Intercollegiate* are significantly different than those in *Arthrex*, or here. The Librarian of Congress—the principal officer who supervises the Copyright Royalty Judges (CRJs) at issue—was much more constrained in her ability to direct and supervise the CRJs than the Director. The governing statute grants CRJs broad discretion over rate-making. *See* 17 U.S.C. § 802(f)(1)(A)(i) (stating that "[CRJs] shall have full independence in making" numerous copyright rate-related decisions). The

Librarian "ap-prov[es] the CRJs' procedural regulations, . . . issu[es] ethical rules for the CRJs, [and] . . . oversee[s] various logistical aspects of their duties," such as publishing CRJs' decisions and providing administrative resources. *Intercollegiate*, 684 F.3d at 1338. In fact, it appears the only way the Librarian can exercise substantive control over the CRJs' ratemaking decisions is indirectly through the Register of Copyrights, whom she, not the President, appoints. See 17 U.S.C. § 701(a). The Register corrects any legal errors in the CRJs' ratemaking decisions, 17 U.S.C. § 802(f)(1)(D), and provides written opinions to the CRJs on "novel question[s] of law," 17 U.S.C. § 802(f)(1)(B), or when the CRJ requests such an opinion. 17 U.S.C. § 802(f)(1)(A)(ii). But the CRJs may not consult with the Register about a question of fact. 17 U.S.C. § 802(f)(1)(A)(i). The Librarian therefore exerts far less control over CRJs than the Director can over APJs using all the powers of direction and supervision discussed in Section I A, *supra*.

The ill-suited comparison to *Intercollegiate* in *Arthrex* again highlights how the unique powers of direction and supervision in each case should be viewed in totality, rather than as discrete categories weighing in favor of inferior officer status or not. In particular, by breaking up the analysis into three discrete categories—Review, Supervision, and Removal—the *Arthrex* panel overlooks how the powers in each category impact each other. Again, for ex-ample, whereas ex post the Court of Appeals for the Armed Forces has more power to review the Court of Criminal Ap-peals judges' decisions than the Director has to review a Board decision, neither

the JAG nor the Court of Appeals for the Armed Forces have the Director's ex ante control, such as the power to decide whether to hear a case at all or to issue binding guidance on how to apply the law in a case. Viewed through this integrated lens, I believe APJs comfortably fit with prior Supreme Court precedent that has never found a principal officer in a challenged position to date.

C

Finally, to the extent that the *Arthrex* panel decision is based on the lack of review along with perceived impermissible restrictions on removal of APJs, I believe it misapprehends the applicable efficiency of the service standard that protects APJs. The efficiency of the service standard al-lows discipline and removal for "misconduct [that] is likely to have an adverse impact on the agency's performance of its functions." *See Brown v. Dep't of the Navy*, 229 F.3d 1356, 1358 (Fed. Cir. 2000). To be sure, the efficiency of the service standard does not allow discipline or removal of APJs "without cause," as in *Edmond*. *See Arthrex*, 941 F.3d at 1333. But neither the Supreme Court nor this court has required that a civil servant be removable at will to qualify as an inferior officer. To the contrary, the Supreme Court and this court have upheld for-cause removal limitations on inferior officers. *See, e.g., Morrison v. Olson*, 487 U.S. 654, 692–93 (1988) (holding that the "good cause" restriction on removal of the independent counsel, an inferior officer, is permissible); *Masias*, 634 F.3d at 1294 (stating that the Court of Federal Claims can remove special masters for "incompetency, misconduct, or neglect of duty or for physical or mental disability or for other

good cause shown"). *See also Free Enterprise*, 561 U.S. at 494 (explaining that the Court previously "adopted verbatim the reasoning of the Court of Claims, which had held that when Congress ' "vests the appointment of inferior officers in the heads of Departments[,] it may limit and restrict the power of removal as it deems best for the public interest' " (alteration in original) (quoting *United States v. Perkins*, 116 U.S. 483, 485 (1886) (itself quoting *Perkins v. United States*, 20 Ct. Cl. 438, 444 (1885)))).

The efficiency of the service standard allows supervisors to discipline and terminate employees for arguably even a wider range of reasons than the standards above, including failure or refusal to follow the Director's policy or legal guidance. Together with the significant authority the Director wields in directing and supervising APJs' work, the ability to remove an APJ on any grounds that promote the efficiency of the service supports finding that APJs are inferior officers.

II

Assuming for the sake of argument that APJs are principal officers, a remedy is required to cure the constitutional violation arising from their present appointment scheme. However, I do not believe that the remedy pro-posed by the *Arthrex* panel comports with congressional in-tent as evidenced by the employment protections provided to APJs and their predecessors for over thirty years. The *Arthrex* panel makes APJs removable at will by partially severing 35 U.S.C. § 3(c) as it applies Title 5's removal protections to APJs. *Arthrex*, 941 F.3d at 1337–38. I question whether Congress would have wanted to leave APJs with-out the removal

protections of Title 5. But, given the high standard for finding non-severability, I cannot say that the Arthrex panel's remedy was improper.

A

Before proceeding to the traditional severance analysis, I must note several concerns about the panel's purported "severance." In traditional severance cases, both the unconstitutional language being severed and the remaining language are usually part of one statute enacted at the same time. In what appears to be a smaller number of cases, an unconstitutional amendment was severed from the original statute. *E.g., Reitz v. Mealey*, 314 U.S. 33, 38–39 (1941), *overruled in part on other grounds by Perez v. Campbell*, 402 U.S. 637 (1971). But here the "severance" is far more convoluted—to the extent that I question whether "severance" is even the appropriate characterization of the *Arthrex* remedy.

A court may sever the application of a particular statute without striking language explicitly. *See, e.g., Nat'l Fed'n of Indep. Bus. v. Sebelius,* 567 U.S. 519, 586 (2012) (invalidating the application of a statute to cure a constitutional defect). But the *Arthrex* panel did not simply sever the application of 35 U.S.C. § 3(c) to APJs. It severed § 3(c)'s application of Title 5 protections, but only with respect to Title 5's removal protections, and only to APJs. See Arthrex, 941 F.3d at 1337–38. In doing so, it severed the application of a separate statute, indeed, a section in a separate title of the United States Code. *Id*. Further, the Title 5 employment protections afforded by 35 U.S.C. § 3(c) al-ready existed when Congress significantly amended other portions of Title 35, but made no changes to § 3(c), with the

America Invents Act in 2011. *See infra* Section II C. I question whether it is appropriate to solve the alleged constitutional infirmity at issue in *Arthrex* and in this case by severing the application of a statute that Congress left un-touched in its most recent revision, the substance of which had applied in various forms for over 30 years. *See infra* Section II B.

B

When faced with an unconstitutional statute, we must determine whether severing the offending portion is possible. To do so, we must determine if the remaining statute "will function in a manner consistent with the intent of Congress." *Alaska Airlines, Inc. v. Brock*, 480 U.S. 678, 685 (1987) (emphasis removed).

The question of severability is a weighty one and the bar for finding an unconstitutional provision non-severable is high. We "must refrain from invalidating more of the statute than is necessary. Indeed, we must retain those portions of the Act that are (1) constitutionally valid, (2) capable of 'functioning independently,' and (3) consistent with Congress' basic objectives in enacting the statute." *United States v. Booker*, 543 U.S. 220, 258–59, (2005) (internal citations omitted).

Because the statute as severed by *Arthrex* can function independently and is constitutionally valid, the key question is whether the statute as excised "remains consistent with Congress' initial and basic . . . intent." *Id.* at 264. Here, I question whether the *Arthrex*-excised statute does so. Congress afforded federal employment protections to

APJs and their predecessors for over thirty years. And it seems unlikely to me that Congress, faced with this Appointments Clause problem, would have chosen to strip APJs of their employment protections, rather than choose some other alternative. However, because the bar for non-severability is so high, and Congress can, at the end of the day, make another legislative choice if it disagrees with the outcome here, I reluctantly conclude that § 3(c) can be severed as it applies to the removal protections for APJs.

To be sure, I do not question the ability to sever an un-constitutional provision lightly. But our touchstone must remain the intent of Congress, and in this case, Congress has maintained federal employment protections for USPTO officers and employees, including APJs and their predecessors, from 1975 to today. This long-standing statutory protection leads me to believe that Congress intended for APJs to have removal protections, such as those incorporated through Title 5 in 35 U.S.C. § 3(c), regardless of changes made to the Board's duties in the AIA.

C

As the *Arthrex* panel noted, examiners-in-chief—"the former title of the current APJs"—were in fact nominated by the President and confirmed by the Senate until 1975. *Arthrex*, 941 F.3d at 1344. *See also* 35 U.S.C. § 3 (1952). But the 1975 amendment did not simply remove Presidential nomination and Senate confirmation; it instead pro-vided for the appointment of examiners-in-chief (1) by the Secretary of Commerce (2) "under the classified civil ser-vice." An Act To Amend Title 35, United States

Code, "Patents", and For Other Purposes, Pub. L. No. 93–601, secs. 1–2, §§ 3, 7, 88 Stat. 1956, 1956 (1975) (codified as amended at 35 U.S.C. §§ 3, 7 (1976)). This amendment provided federal employment protections to examiners-in-chief. *See, e.g., Arnett v. Kennedy*, 416 U.S. 134, 150–51 (1974), *overruled in part on other grounds by Cleveland Bd. of Educ. v. Loudermill*, 470 U.S. 532 (1985) (explaining that the Lloyd-LaFollette Act's "efficiency of the service" standard governed the dismissal of a competitive civil service employee); *Cole v. Young*, 351 U.S. 536, 543 (1956) (describing dismissal of federal employees as governed by "general personnel laws," such as the Lloyd-LaFollette Act's "efficiency of the service" standard).

Two reasons for this change appear in the legislative history. First, due to the growing number of examiners-in-chief, Presidential nomination and Senate confirmation posed a "burden." H.R. REP. NO. 93-856, at 2 (1974). In an early case discussing the Appointments Clause, the Supreme Court said that this was exactly the reason for providing for appointment of inferior officers by people other than the President. *United States v. Germaine*, 99 U.S. 508, 509–10 (1878). Second, the position of examiner-in-chief "requir[es] unique legal and technical qualifications and experience." An Act To Amend Title 35, United States Code, "Patents", and For Other Purposes: Hearing on S. 645, H.R. 5237, S. 1253 and S.1254 Before Subcomm. No. 3 of the H. Comm. on the Judiciary, 92d Cong. 28–29 (1974) (letter from William N. Letson, Acting General Counsel of the Dep't of Commerce, to Emanuel Celler, Chairman of the H. Comm. on the Judiciary).

In making this change, Congress implicitly recognized that APJs be-longed in the civil service, where expertise and nonpartisan decision-making are expected of all civil servants. Indeed, such ideas motivated the passage of the Civil Service Re-form Act (CSRA) only three years after Congress provided for the appointment of APJs through the civil service system. *Lovshin v. Dep't of Navy*, 767 F.2d 826, 832 (Fed. Cir. 1985) (citing the Senate's discussion of the public's right to a government that is both "efficient and effective" and "impartially administered").

Congress then maintained these federal employment protections through several amendments over more than three decades. In 1985, Congress amended 35 U.S.C. § 7, creating the Board of Patent Appeals and Interferences (BPAI) from the existing Board of Appeals, and again pro-vided that the examiners-in-chief "shall be appointed to the competitive service."[7] Patent Law Amendment Acts of 1984, Pub. L. 98–622, title II, sec. 201, § 7(a), 98 Stat. 3383, 3386 (1984) (codified as amended at 35 U.S.C. § 7 (1988)). Though the 1978 CSRA replaced the Lloyd-LaFollette Act between the 1975 and 1985 amendments to 35 U.S.C. § 7, the CSRA maintained the "efficiency of the service" standard for discipline and dismissal of federal employees in the competitive service. 5 U.S.C. § 7513 (1978). *See also Cornelius v. Nutt*, 472 U.S. 648, 669 (1985) ("The statutory phrase 'such cause as will promote the

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[7] For the Appointments Clause analysis here, I treat the terms "competitive service" and "classified civil service" as interchangeable. *See, e.g.*, 5 U.S.C. § 2102(c) (2018) ("As used in other Acts of Congress, 'classified civil service' or 'classified service' means the 'competitive service[.]'").

efficiency of the ser-vice' pre-dates the Civil Service Reform Act's recognition of federal sector collective bargaining.") (Marshall, J., dissenting).

In 1999, Congress made four changes significant here. First, Congress modified the statutory language governing the BPAI, moving the Board's governing language from § 7 to its current location in § 6. See Patent and Trademark Office Efficiency Act, Pub. L. 106–113, ch. 1, sec. 4717, 113 Stat. 1501, 1501A-580 (1999) (codified at 35 U.S.C. § 6 (2000)). Second, it introduced the terminology of administrative patent judge, in place of examiners-in-chief. *Id*. at 1501A-580–81. Third, Congress removed the previous language appointing examiners-in-chief under the competitive service, but added the current § 3(c), giving Title 5 protections to USPTO employees and officers. *Id*. at sec. 4713, § 3(c), 113 Stat. at 1501A-577 (codified as amended at 35 U.S.C. § 3(c) (2000)). This meant that even though their title changed, APJs remained subject to discipline or dismissal subject to the efficiency of the service standard. *See* 5 U.S.C. § 7513 (2000). Fourth, the amendment transferred the power to appoint APJs from the Secretary of Commerce to the Director. Patent and Trademark Office Efficiency Act, Pub. L. 106–113, ch. 1, sec. 4717, 113 Stat. 1501, 1501A-581 (1999) (codified at 35 U.S.C. § 6(a) (2000)).

This fourth change is particularly significant because only a few years later, Congress explicitly considered the constitutionality of this choice—whether APJs were employees that could be appointed by the Director or officers that must be appointed by the Secretary of Commerce. Congress

chose the latter. Consideration of this issue was prompted by an intellectual property law scholar's suggestion in 2007 that APJs were inferior officers, not employees, and therefore must be appointed by the President, a Court of Law, or the Head of a Department. *See* John F. Duffy, *Are Administrative Patent Judges Unconstitutional?,* 2007 PATENTLY-O PAT L.J. 21, 25 (2007). Congress responded swiftly, amending the law in 2008 to give the power to appoint APJs back to the Secretary of Commerce. Patent and Trademark Administrative Judges Appointment Authority Revision, Pub. L. 110–313, sec. 1, § 6, 122 Stat. 3014, 3014 (2008) (codified as amended at 35 U.S.C. § 6(a) (2012)). While some legislators viewed the fix as un-necessary, none suggested that APJs were in fact principal officers appointable only by the President. *Compare* 154 Cong. Rec. H7234 (daily ed. Jul. 29, 2008 edition) (statement of Rep. King) ("[A] straightforward reading of article II, section 2, which I strongly endorse, suggests the 1999 authority that Congress bestowed on the Patent and Trademark Office Director to appoint administrative law judges is unconstitutional, inconsistent with article II, section 2. Instead, this right is more properly reserved for . . . the Secretary of Commerce . . . ."), *with id.* (statement of Rep. Cohen) ("We firmly believe that appointments made by the Director are constitutional."). That Congress explicitly considered the constitutionality of APJ appointments just four years before passing the AIA, and confirmed their appointment by the Head of a Department, strongly suggests that Congress believed APJs were inferior officers in 2000, 2007, and 2011, and thus, could be constitutionally appointed by the Secretary, even

with restrictions on their removal.

Finally, though Congress made significant changes to Title 35 through the AIA, it did not modify § 3(c)'s application of Title 5 protections to USPTO employees and officers.[8] 35 U.S.C. § 3(c) (2012). Yet again, APJs remained subject to the efficiency of the service removal standard applicable to many federal employees.

Further confirmation regarding Congressional intent comes from the fact that § 3 provides specific, and limited, removal procedures for the Director and the Commissioner for Patents, as opposed to all other officers and employees subject to § 3(c). The Director may be removed only by the President. 35 U.S.C. § 3(a)(4). The Commissioner may be removed "for misconduct or nonsatisfactory performance" under her performance agreement, "without regard to the provisions of title 5." 35 U.S.C. § 3(b)(2)(C). That Congress described specific removal procedures for these two positions strongly implies it intended that all other USPTO employees and officers enjoy the Title 5 protections provided in § 3(c).

Given this unbroken line of federal employment protection afforded to APJs and their predecessors for over three decades, I question whether severing § 3(c)'s Title 5 removal protections for APJs "remains consistent with Congress' initial and basic . . . intent." *Booker*, 543 U.S. at 264. My concerns are not

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[8] The AIA did amend 35 U.S.C. § 3(b), *see* Leahy-Smith America Invents Act, Pub. L. 112-29, sec. 21, § 3(b), 125 Stat. 284, 336 (2011) (governing the Director's ability to fix pay for APJs), and 35 U.S.C. § 3(e)(2), *id.* at sec. 20 § 3(e)(2), 125 Stat. at 334 (technical amendment changing "this Act" to "that Act").

alleviated by the *Arthrex* panel's focus on Congress's intent as it pertained to the importance of *inter partes* review, without considering why Congress chose to provide Title 5 employment protections to APJs for decades. *See Arthrex*, 941 F.3d at 1337–38.

D

Finally, I am mindful of the Supreme Court's guidance that:

> Our ability to devise a judicial remedy that does not entail quintessentially legislative work often de-pends on how clearly we have already articulated the background constitutional rules at issue and how easily we can articulate the remedy. . . . But making distinctions in a murky constitutional con-text, or where line-drawing is inherently complex, may call for a 'far more serious invasion of the legislative domain' than we ought to undertake.

Ayotte v. Planned Parenthood of N. New England, 546 U.S. 320, 329–30 (2006) (quoting *United States v. Nat'l Treasury Emps. Union*, 513 U.S. 454, 479 n.26 (1995)). Given the limited extent of Appointments Clause jurisprudence and Congress's repeated decisions to provide federal employment protections to APJs for decades, I am particularly concerned that *Arthrex's* remedy constitutes an unwise invasion of the legislative domain.

I recognize that the *Arthrex* panel considered several potential fixes and chose the one it viewed both as constitutional and minimally disruptive. But removing long-standing employment protections from hundreds of APJs is quite disruptive. Given no

clear evidence that Congress would have intended such a drastic change, I would defer to Congress to fix the problem. This is a legislative problem best left to a legislative solution. Congress faces fewer constraints than we do in fixing an unconstitutional statute. For example, Congress might choose to: grant the Director unilateral review over all Board decisions; make the Chief PTAB Judge a presidential appointee and grant her review of all Board decisions; provide for review of Board decisions by a panel of three Presidential appointees at the USPTO (having created at least two such positions in addition to the Director); or provide for presidential appointment of all APJs.

In sum, I believe the Director currently exercises sufficient oversight and supervision of APJs to render them inferior officers under the Appointments Clause. But if APJs must be viewed as principal officers, I question curing the ensuing constitutional violation by removing their Title 5 removal protections because I believe it conflicts with Congress's intent.

APPENDIX C

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED.,
Appellant,
v.
KINGSTON TECHNOLOGY COMPANY, INC.,
Appellee

ANDREI IANCU, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1202

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2016-01622.

ORDER

PER CURIAM.

In light of this court's decision in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019), and the fact that Polaris Innovations Limited raised an Appointments Clause challenge in its opening brief in the above captioned case,

IT IS ORDERED THAT:

(1) The oral argument scheduled for March 2, 2020 is cancelled and the case is removed from the calendar.

(2) The Patent Trial and Appeal Board's decision in No. IPR2016-01622 is vacated and the case is remanded to the Board for proceedings consistent with the court's decision in *Arthrex*.

FOR THE COURT

January 27, 2020
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

APPENDIX D

Trials@uspto.gov Paper 8
571-272-7822 Entered: February 15, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE
PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,
v.
POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01621
Patent 6,428,057 B1

Before SALLY C. MEDLEY, JEAN R. HOMERE, and KEN B. BARRETT, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–17 of U.S. Patent No. 6,438,057 B1 (Ex. 1001, "the '057 patent"). Paper 3 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 8 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108.

Upon consideration of the Petition and Preliminary Response, we conclude the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–17 of the '057 patent.

A. Related Matters

The parties state that the '057 patent is the subject of a pending lawsuit in the Central District of California Southern Division that includes assertions against Petitioner. Pet. 2; Paper 5 (Patent Owner's Mandatory Notice), 1; Ex. 1002.

B. The '057 Patent

The '057 patent is directed to a method and system for refreshing the contents of a dynamic random access memory (DRAM) array. Ex. 1001, 1:5–7. In particular, the temperature of the DRAM array is utilized to adjust a refresh rate at which the contents of the DRAM array are updated. *Id.* at 1:7–10. Figure 3 of the '057 patent is reproduced below:

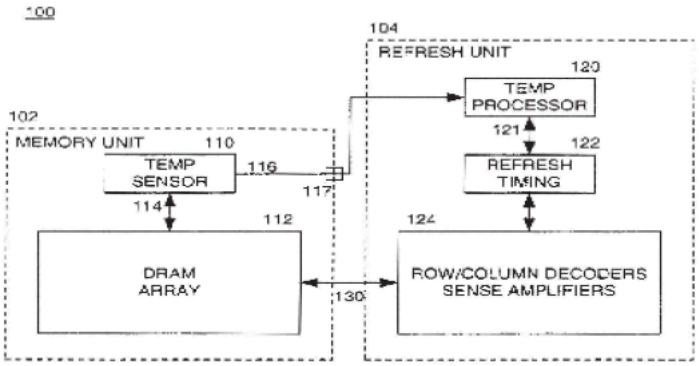

FIG. 3

Figure 3 illustrates system 100 for storing data in DRAM array 112. *Id.* at 4:11–12. In particular, Figure 3 depicts memory unit 102 containing temperature sensor 110 coupled to DRAM array 112, wherein memory unit 102 is connected to refresh unit 104 containing temperature processor 120 coupled to refresh timing 122 and row/column decoders sense amplifiers 124. *Id.* at 4:12–30. According to the '057 patent, "the DRAM array 112 may be implemented on a semiconductor chip and the temperature sensor 110 may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip." *Id.* at 4:22–26.

More specifically, in system 100 illustrated in Figure 3, upon receiving signal 116 from temperature sensor 110 indicating a temperature sensed from DRAM array 112, refresh unit 104 produces refresh signal 130 to refresh DRAM array 112 at a rate that varies in response to received

temperature signal 116. *Id.* at 4:30–32. Preferably, DRAM array 112 is refreshed at a rate that decreases as the temperature of DRAM array 112 decreases. Conversely, DRAM array 112 is refreshed at a rate that increases as the temperature of DRAM array 112 increases. *Id.* at 4:33–37. Further, according to the '057 patent, "the temperature sensor 110 and the DRAM array 112 are preferably disposed in a semiconductor package where the package includes at least one connection pin 117 operable to provide the signal on line 116 to external circuitry, such as the refresh unit 104." *Id.* at 4:49–53. "[T]he temperature sensor 110 preferably includes at least one diode 140 having a forward voltage drop that varies as a function of the temperature of the DRAM array 112." Ex. 1001 at 5:17–20.

C. Illustrative Claim

Petitioner challenges claims 1–17 of the '057 patent. Pet. 9. Claims 1, 13, and 16 are independent claims. Claims 2–12 depend either directly or indirectly from claim 1. Claims 14 and 15 depend either directly or indirectly from claim 13. Claim 17 depends from claim 16. *Id.* at 5:60–8:13.

Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

1. An apparatus, comprising:

a semiconductor package including at least one connection pin;

at least one dynamic random access memory (DRAM) array disposed within the package; and

> at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array, and coupled to the at least one connection pin such that the signal may be provided to external circuitry,
>
> wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

Id. at 5:60–6:7.

Independent claim 13 is similar to claim 1, except that it includes a DRAM chipset comprising a "DRAM chip including a DRAM array and at least a temperature sensor" and one "refresh chip operable to refresh the DRAM array." *Id*. at 6:59–7:6. Independent claim 16 is similar to claim 1, except that it sets forth a method for refreshing contents of a DRAM array at a rate that varies proportionally in response to temperature increases/decreases of the DRAM array. *Id*. at 8:1–9.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–17 are unpatentable based on the following grounds (Pet. 9–10):

Reference(s)	Basis	Challenged Claims
Atkinson[1]	§ 103(a)	1-17
Atkinson and	§ 103(a)	1, 3, 5-9, 12, 13,

[1] US 6,134,167, issued Oct. 17, 2000 (Ex. 1010) ("Atkinson").

Broadwater et al.[2]		and 16
Atkinson, Broadwater, and Miller et al.[3][4]	§ 103(a)	2, 4, 10, 11, 14, 15, and 17
Tillinghast et al.[5] and Broadwater	§ 103(a)	1-17
Kodama[6] and Lee et al.[7] or Broadwater	§ 103(a)	1-17

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b).

Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Patent Owner contends that because Petitioner

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[2] US 4,970,497, issued Nov. 13, 1990 (Ex. 1006) ("Broadwater").
[3] US 3,812,717, issued May 28, 1974 (Ex. 1015) ("Miller").
[4] Although Miller is omitted from Petitioner's summary of asserted grounds, it is nevertheless relied upon in Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17. *See, e.g.*, Pet. 20. We, therefore, treat Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17 based upon Atkinson, Broadwater, and Miller from the statement as a separate ground of unpatentability.
[5] US 5,278,796, issued Jan. 11, 1994 (Ex. 1009) ("Tillinghast").
[6] US 3,851,316, issued Nov. 26, 1974 (Ex. 1004) ("Kodama").
[7] US 5,229,970, issued July 20, 1993 (Ex. 1011) ("Lee").

has not provided in the Petition how each of the challenged claims is to be construed, but instead advises the Board that the claims are to be construed according to their broadest reasonable interpretation, Petitioner has failed to demonstrate a scope of the claimed invention that permits the Board to apply the asserted references to the claims. Prelim. Resp. 5, 8. Further, Patent Owner contends that because Petitioner previously argued in the companion district court litigation that eight different claim terms are indefinite and cannot be construed, Petitioner cannot now request the Board to construe those claim terms according to their broadest reasonable interpretation ("BRI"). *Id.* at 5–7. Patent Owner therefore submits that Petitioner has failed to meet its burden to demonstrate, with reasonable certainty, the scope of the claims to which the Board is to apply the alleged prior art. *Id.* at 7–9.

As set forth above and as correctly noted by the parties, we construe claim terms in an unexpired patent according to the broadest reasonable interpretation. Pet. 11 (citing *Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016); Prelim. Resp. 8. Neither party argues that a claim term is indefinite, and we are not persuaded by Patent Owner's reference to Petitioner's prior allegation of indefiniteness of certain claim terms in the district court proceeding that any of those terms are indefinite. Further, neither party proffers a construction of, or otherwise disputes the meaning of, any of the claim terms. We determine, at this juncture of the proceeding, that it is not necessary to provide any express interpretation of the claim

terms. Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

B. Asserted Obviousness over Atkinson and Broadwater

Petitioner contends claims 1, 3, 5–9, 12, 13, and 16 are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater. Pet. 29–32 (referencing *id.* at 12–28). Relying on the declaration of Dr. Vivek Subramanian, Petitioner explains how the proposed combination of references discloses all of the claim limitations. *Id.* at 12–19, 23–32 (citing Ex. 1005).

1. Atkinson

Atkinson describes a technique for reducing the consumption of electric power in the main computer memory. Ex. 1010, 1:16–20. In particular, Atkinson discloses a refresh logic device that generates a memory refresh signal having a rate, which varies proportionally with the sensed temperature of the computer memory. *Id.* at 5:61–66, 7:41–44.

Figure 8 of Atkinson is reproduced below.

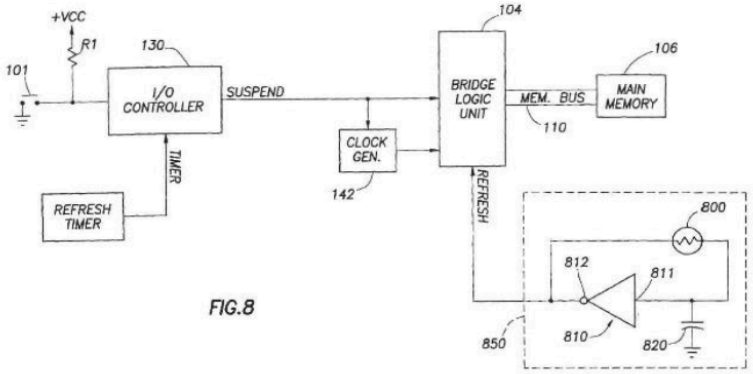

FIG.8

As illustrated in Figure 8 of Atkinson, refresh generator 850 includes thermistor 800, the temperature of which drops upon sensing a decreased temperature of main memory 106 to thereby produce a decrease of the rate of the refresh signal. *Id*. at 22:39–65. "Accordingly, the refresh temperature of the thermistor 800 represents the temperature of the memory storage logic 930, and the refresh frequency decreases approximately in proportion to the decrease in the temperature of the memory storage logic 930." *Id*. at 24:11–17. Conversely, when the temperature of thermistor 800 increases upon sensing an increased temperature of main memory 106, refresh generator 850 increases the rate of the refresh signal. *Id*. at 7:41–44, 21:38–39. Atkinson also discloses an alternative embodiment in which refresh generator 950, including thermistor 800, is integrated in main memory 906. *Id*. at 23:37–40, 24:11–13, 24:22–23, Fig. 9.

Atkinson further discloses that that main memory 906 is an alternative embodiment of main memory 106 that preferably comprises DRAM

circuitry (*id*. at 23:32–34), but may also be other types of DRAM, such as synchronous DRAM (SDRAM), extended data output DRAM (EDO RAM), and Rambus RAM. *Id*. at 3:38–46, 9:1–5. Main memory 106 is connected to bus 110 to exchange signals therewith. *Id*. at 12:4–7.

2. Broadwater

Broadwater relates to a technique for sensing and reducing the effects of thermal stress on packaged semiconductor chips. Ex. 1006, 1:6–8, Abstract. Figure 1 of Broadwater is reproduced below:

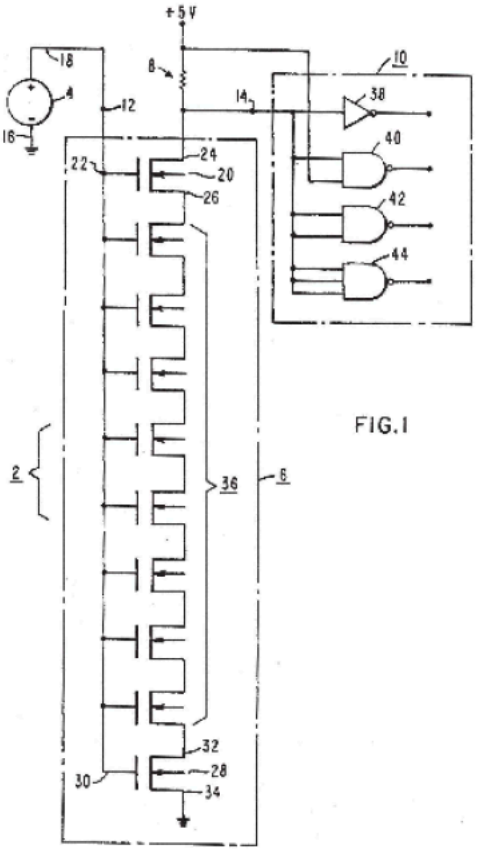

FIG. 1

As depicted in Figure 1 above, Broadwater describes a chip package having thermal stress sensing circuit 6 with input 12 and output 14. *Id.* at 4:3:31–35. The voltage at output 14 varies as a function of input voltage and temperature. *Id.* at 4:39–41, Fig. 2. Output 14 can be routed to gate array 10, as shown, or can be provided to an external pin of the chip package. *Id.* at 4:31–53.

3. Discussion

Petitioner asserts that the combination of

Atkinson and Broadwater discloses the elements of claims 1, 3, 5–9, 12, 13, and 16. Pet. 12–32. We begin our analysis with claim 1. The preamble of claim 1 recites "an apparatus comprising." Ex. 1001, 5:61. Petitioner contends that Atkinson's description of an apparatus containing a main memory with a temperature sensor discloses the preamble of claim 1. Pet. 12.

Claim 1 next recites "a semiconductor package including at least one connection pin." Ex. 1001, 5:62–63. Petitioner contends that Atkinson's description of main memory 106 including any suitable type of memory such as DRAM or any of the special types of DRAM devices (e.g., SDRAM, EDO DRAM, Rambus DRAM) discloses the "semiconductor package" because "one of ordinary skill in the art would know that SDRAM and Rambus DRAM are packaged semiconductor chips." Pet. 13 (citing Ex. 1005 ¶ 41; Ex. 1007, 524; Ex. 1010, 4:31–35, 8:65–9:5). Further, Petitioner asserts that Atkinson's description of main memory 106's connection to bus 110 discloses the "connection pin" because one of ordinary skill would appreciate that "as the main memory is composed of packaged memory chips that receive a variety of bus signals," its "connections to the memory bus 110 would necessarily require at least one connection pin or it would be obvious to have one." *Id.* at 13–14 (citing Ex. 1010, 12:4–7, 23:32–37, 12:8–12; Ex. 1005 ¶ 42).

Claim 1 also recites "at least one dynamic random access memory (DRAM) array disposed within the package." Ex. 1001, 5:64–65. Petitioner asserts that Atkinson's description of a "computer system where the main memory 106 includes an

array of memory devices such as DRAM" discloses the "package" having disposed therein the DRAM array. Pet. 14 (citing Ex. 1010, Figs. 1, 4A, 5, 7–9, 5:57–62, 8:37–9:15; Ex. 1005 ¶ 43).

Claim 1 further recites "at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array." Ex. 1001, 5:66–6:1. Petitioner asserts Atkinson's description of refresh generator 850, including thermistor 800 that directly senses the temperature of the DRAM, discloses "the temperature sensor . . . in thermal communication with the DRAM array." Pet. 14–16 (citing Ex. 1010, 22:52–62, 22:39–67, 23:32–37, 24:1–26, Fig. 8; Ex. 1005 ¶¶ 44, 45). Further, Petitioner asserts Atkinson describes an alternate embodiment wherein a "voltage controlled oscillator [(VCO)] combined with the temperature sensor could replace the refresh generator," such that "the temperature sensor couples to main memory 106, providing a voltage to the VCO that represents the main memory temperature." Pet. 16 (citing Ex. 1010, 23:5–19). The refresh signal produced by the VCO varies with the temperature of the memory device as sensed by the temperature sensor. Pet. 16–17 (citing Ex. 1010, 6:46–62, 7:46–48).

Claim 1 also recites "coupled to the at least one connection pin such that the signal may be provided to external circuitry." Ex. 1001, 6:2–3. Petitioner asserts that Atkinson describes an on-chip embodiment wherein a temperature sensor coupled directly to main memory 106 provides a voltage to the VCO that represents the main memory temperature. Pet. 17 (citing Ex. 1010, 23:15–17, Fig.

8; Ex. 1005 ¶ 47). According to Petitioner, while the on-chip embodiment described by Atkinson does not disclose providing the temperature signal to an external circuit, such a modification would have been obvious to one of ordinary skill in the art, particularly in view of Broadwater's disclosure of an external pin of a chip package (e.g., DRAM memory chip) for outputting a signal indicative of the chip's temperature. *Id*. (citing Ex. 1005 ¶¶ 47–49); *id*. at 30 (citing Ex. 1006, 4:31–33, 4:49–53; Ex. 1005 ¶¶ 83–84). Further, Petitioner asserts that the ordinarily skilled artisan would have been motivated to combine the cited disclosures of Atkinson and Broadwater because Broadwater's disclosure of adding an external pin to an existing chip package (e.g., Atkinson's DRAM) would help reduce the effects of thermal stress on the DRAM. *Id*. at 31 (citing Ex. 1006, 1:14–29; Ex. 1005 ¶ 85). Additionally, Petitioner concludes that the ordinarily skilled artisan would have recognized that the proposed combination would help maximize power saving during the self-refresh timing sequence. *Id*. (citing Ex 1005 ¶ 86).

Claim 1 also recites "wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases." Ex. 1001, 4:4–7. Petitioner asserts Atkinson describes a refresh logic that reduces the rate of the refresh signal in response to receiving a signal from the temperature sensor indicating a drop in the main memory temperature. Pet. 19 (citing Ex. 1010, 13:13–15, 22:2–7). Conversely, the refresh logic increases the rate of the refresh signal in response to

receiving a signal indicating an increase in the temperature of the main memory. *Id*. (citing 1010, 7:41–44; Ex. 1005 ¶¶ 50–51). According to Petitioner, the refresh frequency increases or decreases in proportion to the increase or decrease in the temperature of the DRAM as a way to achieve the greatest power savings. *Id*. (citing Ex. 1010, 20:53–56, 24:3–17, Fig. 6; Ex. 1005 ¶ 51).

Independent claims 13 and 16 are similar to claim 1. Petitioner has made a showing with respect to claims 13 and 16 similar to its showing with respect to claim 1. *See, e.g.*, Pet. 26–28. To the extent that claims 13 and 16 are different from claim 1, Petitioner has accounted for such differences. We also have reviewed Petitioner's showing with respect to dependent claims 3, 5–9, and 12. *Id*. at 21, 23–26.

Patent Owner argues that Petitioner has not accounted sufficiently for each limitation and has not articulated sufficiently a reason to combine the prior art references. Prelim. Resp. 12–34. We address each argument in turn.

Patent Owner contends that Petitioner does not identify in Atkinson a semiconductor package including a "connection pin," as required by independent claims 1 and 13. *Id*. at 13. This argument is not persuasive. As discussed above, Petitioner reasoned that "[a]s the main memory is composed of packaged memory chips that receive a variety of memory bus signals, one of ordinary skill in the art would appreciate that connections to the memory bus 110 would necessarily require at least one connection pin, or it would be obvious to have one." Pet. 13–14 (citing Ex 1005 ¶¶ 41, 42). Further,

at this stage of the proceeding, Dr. Subramanian's testimony is unrebutted. For the foregoing reasons, we agree, on this record, with Petitioner's reasoning.

Patent Owner contends similarly that Petitioner does not demonstrate that the Atkinson-Broadwater combination includes a connection pin that provides a signal to external circuitry. Prelim. Resp. 31–32. As just discussed, however, we are persuaded, on this record, by Petitioner's argument that the limitation of providing the temperature signal to an external circuit is taught by the proposed combination of Atkinson's on-chip embodiment with Broadwater's an external pin of a chip package (e.g., DRAM memory chip) for outputting a signal indicative of the chip's temperature. Pet. 30.

Further, Patent Owner argues that Petitioner does not provide a motivation to combine Atkinson with Broadwater. *Id.* at 32–34. This argument is unavailing. Petitioner asserts the ordinarily skilled artisan would be motivated to combine the cited disclosures of Atkinson and Broadwater because Broadwater's disclosure of adding an external pin to Atkinson's DRAM would help reduce the effects of thermal stress on the DRAM, and would help maximize power saving during the self-refresh timing sequence. *Id.* at 31 (citing Ex. 1005 ¶¶ 85, 86). At this stage, moreover, Dr. Subramanian's testimony is unrebutted. We are persuaded, on this record, that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Patent Owner also argues that "Petitioner does not provide evidence dictating that the rate 'varies in response to the *signal*,' as [claim 6] requires." Prelim. Resp. 23–26. In particular, Patent Owner argues that the cited portion of Atkinson "may well demonstrate that the rate and the temperature are linked," but does not teach "that it is *the signal* that causes the rate to decrease in proportion to the decrease in temperature." *Id.* at 23 (emphasis added). This argument is not persuasive. The antecedent basis for "the signal" is in claim 1, where Petitioner relies upon Atkinson's teaching of the refresh generator output, which is indicative of the temperature of the DRAM as measured by thermistor 800. Pet. 14–17 (discussing embodiments described in Figures 8 and 9 of Atkinson). In connection with the embodiment of Figure 8, Atkinson teaches explicitly that "[t]he frequency of the refresh signal in this embodiment continuously reduces as temperature decreases, rather than in discrete steps as in prior embodiments. Thus, refresh generator 850 provides a refresh signal that closely follows the temperature/frequency response of curve 600 or any other desired temperature/frequency response curve." Ex. 1010, 22:62–23:1. As a result, we agree with and are persuaded by Petitioner's contentions that Atkinson teaches refreshing the DRAM array at a rate that varies in response to the *signal*, as claim 6 requires, and not merely in response to the temperature of the DRAM array, as Patent Owner suggests.

Patent Owner also argues that Petitioner's contentions with respect to claim 7 are inconsistent with positions taken by Petitioner in the

corresponding district court litigation. Prelim. Resp. 26–27. This argument is not persuasive. As noted above, neither party argues in this proceeding that the term "refresh unit" recited in claim 7 is a means-plus-function term or that it is indefinite. Consequently, Patent Owner's reference to Petitioner's prior construction of "refresh unit" in the district court proceeding is not persuasive. On this record, we are persuaded that Atkinson's voltage controller oscillator (VCO) describes the refresh timing unit. Pet. 23–24.

Patent Owner also argues that Petitioner's contentions with respect to claims 8 and 9 rely on two distinct embodiments of Atkinson without explaining "how or why one would combine the two embodiments." Prelim. Resp. 28. This argument is not persuasive. Although Atkinson describes a first embodiment including refresh generator 850, and another embodiment wherein the refresh generator is replaced with the VCO combined with a temperature sensor, Petitioner does not rely upon the two cited embodiments to describe the limitations claims 8 and 9. Instead, Petitioner relies only upon the latter embodiment to meet the claim limitations. *See* Pet. 24–25. Even if Petitioner relied upon both embodiments to support the assertion of obviousness, such a combination would not necessarily be improper because this ground is based upon obviousness rather than anticipation.

Finally, with respect to claim 13, Patent Owner argues that Petitioner has not identified with sufficient clarity what in Atkinson teaches the recited "DRAM chip," "refresh chip," "connection pin," or "external circuitry." Prelim. Resp. 29–30. We

disagree. As noted above, Petitioner has made a showing with respect to claim 13 similar to its showing with respect to claim 1. *See*, e.g., Pet. 26–28. To the extent that claim 13 is different from claim 1, Petitioner has accounted for such differences. *Id*.

Based on the current record before us, we determine that there is a reasonable likelihood that Petitioner would prevail in establishing that claims 1, 3, 5–9, 12, 13, and 16 are unpatentable over the combination of Atkinson and Broadwater.

C. Asserted Obviousness over Atkinson, Broadwater, and Miller

Petitioner contends claims 2, 4, 10, 11, 14, 15, and 17 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Atkinson, Broadwater, and Miller.[8] Pet. 20–21, 22, 25, 27, 28, and 29–30. Relying on the declaration of Dr. Subramanian, Petitioner explains how the proposed combination of references discloses all of the claim limitations. *Id*. (citing Ex. 1005).

On this record, Petitioner has accounted sufficiently for the limitations of claims 2, 4, 10, 11, 14, 15, and 17. For example, claim 2 depends directly from claim 1 and recites "wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode." Ex. 1001, 6:8–12.

Petitioner asserts that, although the '057 patent includes a diode as a known temperature sensor, it

[8] See supra note 4.

also discloses other known temperature sensors (e.g., thermocouples, thermistors, or any other device that provides an output signal varying as a function of temperature). Pet. 20 (citing Ex. 1001, 2:42–45). Petitioner further asserts that Atkinson similarly discloses the use of such known temperature sensors (e.g., thermocouple or temperature sensing integrated circuit). *Id.* (citing Ex. 1010, 22:21–24; Ex. 1005 ¶¶ 52, 53). Petitioner then contends that, at the time of the invention, measuring a forward voltage drop across a semiconductor diode to thereby read the temperature, as described in Miller, was a well-known use of such a type of temperature sensor. Pet. 20 (citing Ex. 1015, Abstract). Petitioner concludes it would have been obvious to one of ordinary skill in the art to select a diode as a well-known type of temperature sensor for reading the temperature of Atkinson's DRAM. *Id.* at 21 (citing Ex. 1010, 24:63–65; 1005 ¶ 53).

> Likewise, claim 4 depends directly from claim 1, and recites
>
> wherein the at least one temperature sensor includes having a forward voltage drop that varies as a function of the temperature of the DRAM array; the at least one connection pin includes a first pin coupled to an anode of the diode and a second pin coupled to the cathode of the diode; and the signal corresponds to a potential voltage between the first and second pins.

Ex. 1001, 6:17–23.

Petitioner explains, with supporting evidence, that at the time of the invention, "given that the

claim merely recites 'first pin' and 'second pin,' the diode temperature sensor would necessarily be connected to a first pin and a second pin if it were operational." *Id.* at 22 (citing Ex. 1005 ¶ 56). Petitioner further explains that "in such a diode configuration, the signal between the first pin and the second pin would necessarily be the forward voltage drop of the diode, which claim 4 defines as the signal." *Id.* Petitioner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to "modify Atkinson to use a diode configuration as recited in claim 4 (which is essentially the same as the obvious variant in claim 2)." *Id.*

We also have reviewed the Petition with respect to dependent claims 10, 11, 14, 15, and 17, and determine that at this juncture of the proceeding Petitioner has accounted sufficiently for the recited limitations. Pet. 25, 27 and 28.

Patent Owner argues that Petitioner's reliance on "finite alternate types of integrated circuits for detecting temperatures" is a misapplication of KSR because the number of available alternatives is "far from 'small or easily traversed.'" Prelim. Resp. 19–23(citing *Ortho-McNeill Pharmaceutical, Inc., v. Mylan Laboratories,, Inc.*, 520 F.3d 1358, 1364 (Fed. Cir. 2008). This argument is moot in light of Petitioner's alternative reliance upon Miller's diode to measure the temperature of Atkinson's DRAM. Pet. 20.

Patent Owner also argues that Miller is not part of any combination and that no motivation is given by Petitioner to combine Atkinson with Miller.

Prelim. Resp. 22. As discussed above, however, we interpret the ground of unpatentability as including Miller.[9] Petitioner has sufficiently shown, at this stage of the proceeding, that it would have been obvious to use the diode described in Miller to read and measure the temperature of Atkinson's DRAM. Pet. 20–21. On the record before us, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness based on Atkinson, Broadwater, and Miller. *See KSR*, 550 U.S. at 418.

For the foregoing reasons, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that the subject matter of claims 2, 4, 10, 11, 14, 15, and 17 would have been obvious over the combination of Atkinson, Broadwater, and Miller.

D. Remaining Grounds

Petitioner argues that the challenged claims are unpatentable under 35 U.S.C. § 103 as obvious over (1) Atkinson alone; (2) Tillinghast and Broadwater; and (3) Kodama and Lee '970 or Broadwater. Pet. 12–28, 33–61. The Board's rules for AIA *inter partes* proceedings, including those pertaining to institution, are "construed to secure the just, speedy, and inexpensive resolution of every proceeding." 37 C.F.R. § 42.1(b); *accord* 35 U.S.C. §§ 316(b) (regulations for AIA *inter partes* proceedings take into account "the efficient administration of the Office" and "the ability of the Office to timely complete [instituted] proceedings"). Because we institute an *inter partes*

[9] *See supra* notes 3 & 4.

review of these claims based on the grounds discussed above, we exercise our discretion not to institute a review based on these grounds for reasons of administrative expediency to ensure timely completion of the instituted proceeding. *See* 37 C.F.R. § 42.108(a) ("the Board may authorize the review to proceed . . . on all or some of the grounds of unpatentability asserted for each claim"); 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1368 (Fed. Cir. 2016) ("[U]nder [37 C.F.R. § 42.108(a)], it is clear that the Board may choose to institute some grounds and not institute others as part of its comprehensive institution decision.").

III. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claims 1–17 of the '057 patent are unpatentable. At this preliminary stage, we have not made a final determination with respect to the patentability of the challenged claims or any underlying factual or legal issues.

IV. ORDER

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–17 of the '057 patent on the following grounds of unpatentability:

Reference(s)	Basis	Challenged Claims
Atkinson and Broadwater	§ 103(a)	1, 3, 5-9, 12, 13, and 16

Atkinson, Broadwater, and Miller	§ 103(a)	2, 4, 10, 11, 14, 15, and 17

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this decision; and

FURTHER ORDERED that the trial is limited to the grounds identified immediately above, and no other ground is authorized.

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APPENDIX E

Trials@uspto.gov Paper 33
571-272-7822 Entered: January 29, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE
PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,
v.
POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01621
Patent 6,428,057 B1

Before SALLY C. MEDLEY, JEAN R. HOMERE, and KEN B. BARRETT, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(A) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Kingston Technology Company, Inc. ("Petitioner") challenges claims 1–17 ("the challenged claims") of U.S. Patent No. 6,438,057 B1 (Ex. 1001, "the '057 patent"), owned by Polaris Innovations Ltd. ("Patent Owner"). [1] We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.

A. Procedural History

Petitioner filed a Petition requesting an *inter partes* review of claims 1–17 of the '057 patent. Paper 2 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp."). On February 15, 2017, we instituted *inter partes* review of claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson,[2] and Broadwater.[3] Paper 8 ("Inst. Dec."), 17. Further, we instituted *inter partes* review of claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson, Broadwater, and

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[1] Patent Owner identifies Polaris Innovations Ltd., Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 4, 2; Paper 20, 2.

[2] U.S. Patent No. 6,134,167, issued Oct. 17, 2000 (Ex. 1010) ("Atkinson").

[3] U.S. Patent No. 4,970,497, issued Nov. 13, 1990 (Ex. 1006) ("Broadwater").

Miller.[4] *Id*. at 20.

Thereafter, Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp."), to which Petitioner filed a Reply (Paper 21, "Reply"). Pursuant to an Order (Paper 22), Patent Owner filed a listing of alleged statements and evidence in connection with Petitioner's Reply that Patent Owner considered to be beyond the proper scope of a reply. Paper 23. Petitioner filed a response to Patent Owner's listing. Paper 24.

We held a consolidated hearing on November 14, 2017, for this case and related Cases IPR2016-01622 and IPR2016-01623, and a transcript of the hearing is included in the record. Paper 32 ("Tr.").

B. Related Proceedings

The parties state that the '057 patent is the subject of a pending lawsuit in the Central District of California Southern Division that includes assertions against Petitioner. Pet. 2; Paper 4 (Patent Owner's Mandatory Notice), 1; Ex. 1002.

C. The '057 patent (Ex. 1001)

The '057 patent is directed to a method and system for refreshing the contents of a dynamic random access memory (DRAM) array. Ex. 1001, 1:5–7. In particular, the temperature of the DRAM array is utilized to adjust a refresh rate at which the contents of the DRAM array are updated. *Id*. at 1:7–10. Figure 3 of the '057 patent is reproduced below:

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[4] U.S. Patent No. 3,812,717, issued May 28, 1974 (Ex. 1015) ("Miller").

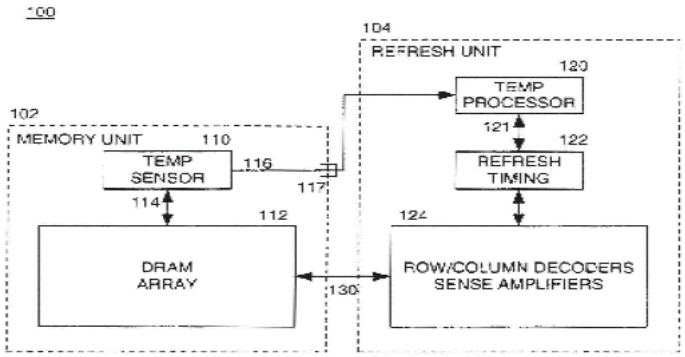

FIG. 3

Figure 3 illustrates system 100 for storing data in DRAM array 112. *Id*. at 4:11–12. In particular, Figure 3 depicts memory unit 102 containing temperature sensor 110 coupled to DRAM array 112, wherein memory unit 102 is connected to refresh unit 104 containing temperature processor 120 coupled to refresh timing 122 and row/column decoders sense amplifiers 124. *Id*. at 4:12–30. According to the '057 patent, "the DRAM array 112 may be implemented on a semiconductor chip and the temperature sensor 110 may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip." *Id*. at 4:22–26.

More specifically, in system 100 illustrated in Figure 3, upon receiving signal 116 from temperature sensor 110 indicating a temperature sensed from DRAM array 112, refresh unit 104 produces refresh signal 130 to refresh DRAM array

112 at a rate that varies in response to received temperature signal 116. *Id*. at 4:30–32. Preferably, DRAM array 112 is refreshed at a rate that decreases as the temperature of DRAM array 112 decreases. Conversely, DRAM array 112 is refreshed at a rate that increases as the temperature of DRAM array 112 increases. *Id*. at 4:33–37. Further, according to the '057 patent, "the temperature sensor 110 and the DRAM array 112 are preferably disposed in a semiconductor package where the package includes at least one connection pin 117 operable to provide the signal on line 116 to external circuitry, such as the refresh unit 104." *Id*. at 4:49–53. "[T]he temperature sensor 110 preferably includes at least one diode 140 having a forward voltage drop that varies as a function of the temperature of the DRAM array 112." *Id*. at 5:17–20.

D. Illustrative Claim

Of the instituted claims, claims 1, 13, and 16 are independent. Claims 2–12 depend from independent claim 1. Claims 14 and 15 depend from independent claim 13. Claim 17 depends from independent claim 16. Independent claim is illustrative of the challenged claims, and is reproduced below:

> 1. An apparatus, comprising:
>
> a semiconductor package including at least one connection pin;
>
> at least one dynamic random access memory (DRAM) array disposed within the package; and
>
> at least one temperature sensor in thermal communication with the DRAM array,

> operable to produce a signal indicative of a temperature of the DRAM array, and coupled to the at least one connection pin such that the signal may be provided to external circuitry,
>
> wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

Ex. 1001, 5:60–6:7.

II. ANALYSIS

A. Claim Construction

The Board interprets claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. See 37 C.F.R. § 42.100(b); see *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In our Decision on Institution, we found no material dispute between the parties as to claim construction in the present proceeding. Inst. Dec. 7.

Patent Owner contends that because Petitioner has not provided in the Petition how each of the challenged claims is to be construed, but instead advises the Board that the claims are to be construed according to their plain and ordinary

meaning, Petitioner has failed to demonstrate a scope of the claimed invention that permits the Board to apply the asserted references to the claims. PO Resp. 13–14. Further, Patent Owner contends Petitioner previously argued in the companion district court litigation that the claim terms "refresh unit" and "refresh timing unit" in claims 6–11 are means plus function recitations with no corresponding structures in the Specification; that the cited claim terms are indefinite and cannot be construed. *Id*. at 16–17. According to Patent Owner, Petitioner cannot now request the Board to construe those claim terms as anything other than means plus function recitations. *Id*. at 17–18. Patent Owner, therefore, submits that Petitioner has failed to meet its burden to demonstrate, with reasonable certainty, the scope of the claims to which the Board is to apply the alleged prior art. *Id*. at 18.

These arguments are not persuasive. Petitioner was not required to make explicit claim constructions for each term of each claim. "It may be sufficient for a party to provide a simple statement that the claim terms are to be given their broadest reasonable interpretation, as understood by one of ordinary skill in the art and consistent with the disclosure." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,764 (Aug. 14, 2012). For this reason, we disagree with Patent Owner's contention that Petitioner's statement that the claim terms be given their plain and ordinary meaning is insufficient. We also are not persuaded by Patent Owner's argument that Petitioner's position regarding its proposed claim constructions in the District Court for dependent claims 6–11 and prior

allegation of indefiniteness of the cited claim terms in the district court proceeding "is a failure to meet its burden of proof." PO Resp. 18. We disagree that Petitioner's alleged inconsistent claim construction positions are fatal to Petitioner. Moreover, we decline Patent Owner's invitation to consider on the merits Petitioner's arguments made in the related District Court proceeding. PO Resp. 18. Here, neither party proffers an explicit construction of, or otherwise disputes the meaning of, any of the claim terms. We determine that it is not necessary to provide any express interpretation of the claim terms. Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

B. Level of Ordinary skill in the Art

Both Petitioner's Declarant, Dr. Vivek Subramanian, and Patent Owner's Declarant, Dr. Joseph Bernstein, contend that a person having ordinary skill in the art at the time of the invention would have had (1) a Master's degree in Electrical Engineering, and (2) two to five years of experience working in the field of semiconductor design. Ex. 1005 ¶ 17, Ex. 2008 ¶ 25.

This definition is consistent with the level of ordinary skill reflected in the prior art references of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect an appropriate level of skill in the art). ; *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). For purposes of this decision, we adopt the undisputed definition of the person of ordinary skill in the art, as set forth

above.

C. The Parties' Post-Institution Arguments

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater. Inst. Dec. 17. Further, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent under 35 U.S.C. § 103(a) are unpatentable over the combination of Atkinson, Broadwater, and Miller. *Id*. at 20. We must now determine whether Petitioner has established by a preponderance of the evidence that the specified claims are unpatentable over the cited prior art. 35 U.S.C. § 316(e).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of the claims against which that prior art is asserted. Based on the preponderance of the evidence before us, we conclude that the prior art identified by Petitioner teaches or suggests all uncontested limitations of the reviewed claims. The limitations of claim 1 and the limitations in the

other challenged claims that Patent Owner contests in the Patent Owner Response are addressed below.

D. Obviousness over the Combination of Atkinson and Broadwater

Petitioner contends that claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater. Pet. 12–32.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Atkinson Overview

Atkinson describes a technique for reducing the consumption of electric power in the main computer memory. Ex. 1010, 1:16–20. In particular, Atkinson discloses a refresh logic device that generates a

memory refresh signal having a rate, which varies proportionally with the sensed temperature of the computer memory. *Id*. at 5:61–66, 7:41–44.

Figure 8 of Atkinson is reproduced below.

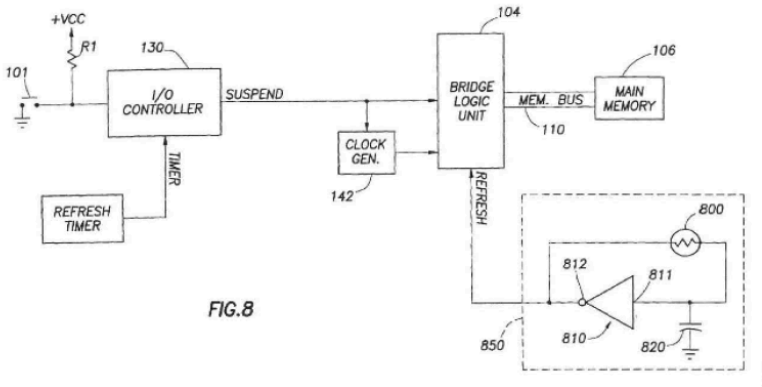

FIG.8

As illustrated in Figure 8 of Atkinson, refresh generator 850 includes thermistor 800, the temperature of which drops upon sensing a decreased temperature of main memory 106 to thereby produce a decrease of the rate of the refresh signal. *Id*. at 22:39–65. "Accordingly, the temperature of thermistor 800 represents the temperature of memory storage logic 930, and the refresh frequency decreases approximately in proportion to the decrease in the temperature of memory storage logic 930." *Id*. at 24:11–17. Conversely, when the temperature of thermistor 800 increases upon sensing an increased temperature of main memory 106, refresh generator 850 increases the rate of the refresh signal. *Id*. at 7:41–44, 21:38–39. Atkinson also discloses an alternative embodiment in which refresh generator 950, including thermistor 800, is integrated in main memory 906. *Id*. at 23:37–40, 24:11–13, 24:22–23,

Fig. 9.

Atkinson further discloses that that main memory 906 is an alternative embodiment of main memory 106 that preferably comprises DRAM circuitry (*id*. at 23:32–34), but may also be other types of DRAM, such as synchronous DRAM (SDRAM), extended data output DRAM (EDO RAM), and Rambus RAM. *Id*. at 3:38–46, 9:1–5. Main memory 106 is connected to bus 110 to exchange signals therewith. *Id*. at 12:4–7.

3. Broadwater Overview

Broadwater relates to a technique for sensing and reducing the effects of thermal stress on packaged semiconductor chips. Ex. 1006, 1:6–8, Abstract. Figure 1 of Broadwater is reproduced below:

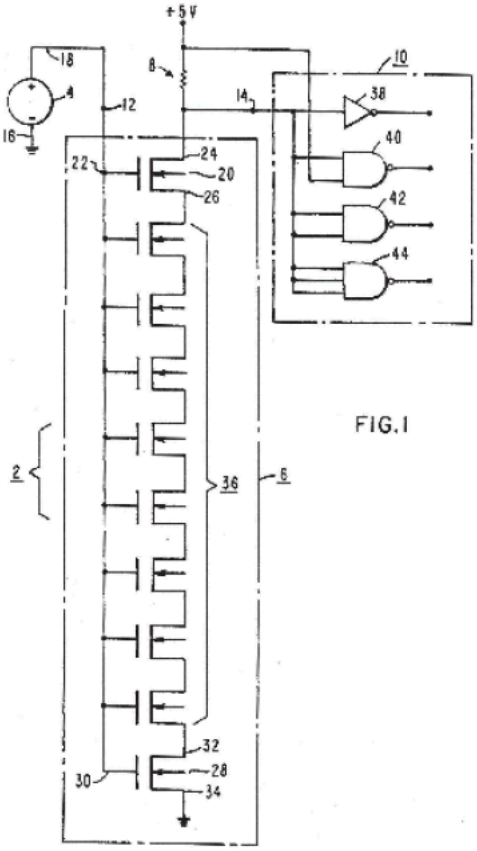

FIG. 1

As depicted in Figure 1 above, Broadwater describes a chip package having thermal stress sensing circuit 6 with input 12 and output 14. *Id.* at 3:35–37, 4:31–35. The voltage at output 14 varies as a function of input voltage and temperature. *Id.* at 4:39–41, Fig. 2. Output 14 can be routed to gate array 10, as shown, or can be provided to an external pin of the chip package. *Id.* at 4:31–53.

4. Petitioner's Positions

Petitioner asserts that the combination of Atkinson and Broadwater discloses the elements of

claims 1, 3, 5–9, 12, 13, and 16. Pet. 12–32. We begin our analysis with claim 1. We have reviewed the Petition, Patent Owner Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers. We are persuaded that the record sufficiently establishes Petitioner's contentions for claims 1, 3, 5–9, 12, 13, and 16.[5]

The preamble of claim 1 recites "an apparatus comprising." Ex. 1001, 5:61. Petitioner contends that Atkinson's description of an apparatus containing a main memory with a temperature sensor discloses the preamble of claim 1. Pet. 12.

Claim 1 next recites "a semiconductor package including at least one connection pin." Ex. 1001, 5:62–63. Petitioner contends that Atkinson's description of main memory 106 including any suitable type of memory such as DRAM or any of the special types of DRAM devices (e.g., SDRAM, EDO DRAM, Rambus DRAM) discloses the "semiconductor package" because "[o]ne of ordinary skill in the art would know that SDRAM and Rambus DRAM are packaged semiconductor chips." Pet. 13 (citing Ex. 1005 ¶ 41; Ex. 1007, 524; Ex. 1010, 4:31–35, 8:65–9:5). Further, Petitioner asserts that Atkinson's description of main memory 106's connection to bus 110 discloses the "connection pin"

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[5] We acknowledge Patent Owner's argument that "Dr. Subramanian's opinions on the ultimate question of obviousness are entitled to no weight" because he is not an attorney. PO Response 28–30. We arrive at the ultimate conclusion regarding obviousness independently and without adopting any purported "lay opinions" on the ultimate issue, *id.* at 28–29.

because one of ordinary skill would appreciate that "[a]s the main memory is composed of packaged memory chips that receive a variety of memory bus signals," its "connections to the memory bus 110 would necessarily require at least one connection pin or it would be obvious to have one." *Id*. at 13–14 (citing Ex. 1010, 12:4–7, 23:32–37, 12:8–12; Ex. 1005 ¶ 42). We are persuaded by Petitioner's showing and find that Atkinson's main memory 106 teaches a packaged semiconductor chip including at least one connection pin.

Claim 1 also recites "at least one dynamic random access memory (DRAM) array disposed within the package." Ex. 1001, 5:64–65. Petitioner asserts that Atkinson's description of a "computer system where the main memory 106 includes an array of memory devices such as DRAM" discloses the "package" having disposed therein the DRAM array. Pet. 14 (citing Ex. 1010, Figs. 1, 4A, 5, 7–9, 5:57–62, 8:37–9:15; Ex. 1005 ¶ 43). We are persuaded by Petitioner's showing and find that Atkinson's description of the main memory packaged in the semiconductor chip teaches a dynamic random access memory.

Claim 1 further recites "at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array." Ex. 1001, 5:66–6:1. Petitioner asserts Atkinson's description of refresh generator 850, including thermistor 800 that directly senses the temperature of the DRAM, discloses "the temperature sensor . . . in thermal communication with the DRAM array." Pet. 14–16 (citing Ex. 1010, 22:52–62, 22:39–67, 23:32–37, 24:1–26, Fig. 8; Ex.

1005 ¶¶ 44, 45). Further, Petitioner asserts Atkinson describes an alternate embodiment wherein a "voltage controlled oscillator [(VCO)] combined with a temperature sensor could replace the refresh generator," such that "***the temperature sensor couples to main memory 106****, providing a voltage to the VCO* ***that represents the main memory temperature***." *Id.* at 16 (citing Ex. 1010, 23:5–19). The refresh signal produced by the VCO varies with the temperature of the memory device as sensed by the temperature sensor. Id. at 16–17 (citing Ex. 1010, 6:46–62, 7:46–48). We are persuaded by Petitioner's showing and find that Atkinson's description of the refresh generator, and alternatively the voltage controlled oscillator combined with the temperature sensor, teaches a sensor coupled to the DRAM array to indicate the temperature of the DRAM array.

Claim 1 also recites "coupled to the at least one connection pin such that the signal may be provided to external circuitry." Ex. 1001, 6:2–3. Petitioner asserts that Atkinson describes an on-chip embodiment wherein a temperature sensor coupled directly to main memory 106 provides a voltage to the VCO that represents the main memory temperature. Pet. 17 (citing Ex. 1010, 23:15–17, Fig. 8; Ex. 1005 ¶ 47). According to Petitioner, while the on-chip embodiment described by Atkinson does not disclose providing the temperature signal to an external circuit, such a modification would have been obvious to one of ordinary skill in the art, particularly in view of Broadwater's disclosure of an external pin of a chip package (e.g., DRAM memory chip) for outputting a signal indicative of the chip's temperature. *Id.* (citing Ex. 1005 ¶¶ 47–49); *id.* at 30

(citing Ex. 1006, 4:31–33, 4:49–53; Ex. 1005 ¶¶ 83–84).

Further, Petitioner asserts that the ordinarily skilled artisan would have been motivated to combine the cited disclosures of Atkinson and Broadwater because Broadwater's disclosure of adding an external pin to an existing chip package (e.g., Atkinson's DRAM) would help reduce the effects of thermal stress on the DRAM. *Id.* at 31 (citing Ex. 1006, 1:14–29; Ex. 1005 ¶ 85). Additionally, Petitioner concludes that the ordinarily skilled artisan would have recognized that the proposed combination would help maximize power saving during the self-refresh timing sequence. *Id.* (citing Ex 1005 ¶ 86). We are persuaded that a person having ordinary skill in the art would have found it obvious to combine the teachings of Atkinson and Broadwater because we agree that transmitting the sensed temperature of the DRAM to an external circuit via an external pin would have been recognized by a person having ordinary skill in the art as resulting in a more efficient system that maximizes power saving by reducing thermal stress on the packaged semiconductor chip.

Claim 1 also recites "wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases." Ex. 1001, 6:4–7. Petitioner asserts Atkinson describes a refresh logic that reduces the rate of the refresh signal in response to receiving a signal from the temperature sensor indicating a drop in the main memory temperature. Pet. 19 (citing Ex. 1010, 13:13–15, 22:2–7). Conversely, the refresh logic

increases the rate of the refresh signal in response to receiving a signal indicating an increase in the temperature of the main memory. *Id.* (citing Ex. 1010, 7:41–44; Ex. 1005 ¶¶ 50–51). According to Petitioner, the refresh frequency increases or decreases in proportion to the increase or decrease in the temperature of the DRAM as a way to achieve the greatest power savings. *Id.* (citing Ex. 1010, 20:53–56, 24:3–17, Fig. 6; Ex. 1005 ¶ 51). We are persuaded by Petitioner's showing and find that Atkinson's description of the refresh logic teaches a mechanism for providing to the DRAM an increased or decreased refresh rate in proportion with the sensed temperature of the DRAM.

Independent claims 13 and 16 are similar to claim 1. Petitioner has made a showing with respect to claims 13 and 16 similar to its showing with respect to claim 1. *See, e.g.*, Pet. 26–28. To the extent that claims 13 and 16 are different from claim 1, Petitioner has accounted for such differences. We also have reviewed Petitioner's showing with respect to dependent claims 3, 5–9, and 12. *Id.* at 21, 23–26. Notwithstanding Patent Owner's arguments, which we have considered and which we address below, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, as set forth above, that claims 1, 3, 5–9, 12, 13, and 16 are unpatentable as obvious over the combination of Atkinson and Broadwater.

5. Patent Owner's Assertions Concerning the References

Patent Owner argues that the challenged claims would not have been obvious over the combination of

Atkinson and Broadwater for the following reasons: (a) "Petitioner does not demonstrate a proper motivation to modify Atkinson to add Broadwater's 'connection pin' to provide a temperature indicative signal to 'external circuitry,'" as recited in challenged claims 1–17 (PO Resp. 32–53 (emphasis omitted)); (b) "Petitioner has failed to show it was obvious to modify Atkinson to add the 'diode' limitations," as recited in dependent claims 2, 4, 10, 11, 14, and 15 (*id*. at 19–27, 53–57 (emphasis omitted)); and (c) "Petitioner has failed to point out where the 'refresh unit' . . . and 'refresh timing unit' . . . limitations are found," as recited in dependent claims 6–11, and 7–11 respectively (*id*. at 57–60). We address each argument in turn.[6]

a. The Allegation that Petitioner Does Not Demonstrate a Proper Reason to Modify Atkinson to

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[6] Patent Owner lists several portions of Petitioner's Reply and evidence as being allegedly beyond the scope of what can be considered appropriate for a reply. *See* Paper 23. We have considered Patent Owner's listing, but disagree that the cited portions of Petitioner's Reply and reply evidence are beyond the scope of what is appropriate for a reply. Replies are a vehicle for responding to arguments raised in a corresponding patent owner response. Petitioner's arguments and evidence that Patent Owner objects to (*id*. at 1) are not beyond the proper scope of a reply because we find that they fairly respond to Patent Owner's arguments raised in Patent Owner's Response. *See Idemitsu Kosan Co., Ltd. v. SFC Co. Ltd*., 870 F.3d 1376, 1381 (Fed. Cir. 2017) ("This back-and-forth shows that what Idemitsu characterizes as an argument raised 'too late' is simply the by-product of one party necessarily getting the last word. If anything, Idemitsu is the party that first raised this issue, by arguing—at least implicitly—that Arakane teaches away from non-energy-gap combinations. SFC simply countered, as it was entitled to do.").

Add Broadwater's "Connection Pin" to Provide a Temperature Indicative Signal to "External Circuitry" (claims 1–17)

Independent claim 1 recites, in relevant part, "at least one connection pin such that the signal may be provided to external circuitry." Independent claim 13 recites, in relevant part, "at least one connection pin operable to provide the signal to external circuitry." Independent claim 16 recites, in relevant part, "outputting a signal indicative of the temperature of the DRAM array to external circuitry." Patent Owner presents four sub-arguments: (i) "The teachings of Atkinson and Broadwater discourage the combination" (PO Resp. 37–42 (emphasis omitted)); (ii) "Even if Atkinson and Broadwater were not contrary to the Patent's teaching, there is no reason to combine them to make the specific invention claimed" (*id*. at 42–47 (emphasis omitted)); (iii) "The proposed Atkinson-Broadwater combination would require extensive modifications of Atkinson to practice the claims" (*id*. at 48–50 (emphasis omitted)); and (iv) "Petitioner and its declarant wave aside the references' disclosures and rely on generalities and offhand comments in each reference" (*id*. at 50–53 (emphasis omitted)). We address each in turn.

i. Whether the teachings of Atkinson and Broadwater Discourage the Combination.

Patent Owner argues that "[t]here is no motivation to couple Atkinson's onboard sensor to a connection pin such that the temperature indicative signal may be provided to external circuitry, because in Atkinson all external circuitry, particularly any

that might affect the DRAM refresh rate, is expressly turned off." PO Resp. 37 (citing Ex. 1010, 4:54–59, 6:6–10, 11:4–16). Specifically, Patent Owner argues that every embodiment disclosed in Atkinson is focused on performing the refresh operation during system sleep with all external logic/circuitry outside of the DRAM module off. *Id*. According to Patent Owner, modifying Atkinson's onboard module in its sleep state (during which the rate of temperature decreases to control the DRAM refresh rate) to operate with an external circuitry in active state, would go against the thrust of Atkinson. *Id*. (citing Ex. 2008 ¶ 60). Patent Owner stresses that Atkinson's "on-chip" embodiment with the temperature sensor in thermal communication with the array was designed to be self-contained to include the temperature sensing refresh generator within main memory 906. *Id*. at 38 (citing Ex. 1010, 24:22– 23, 24:23–27; Ex. 2008 ¶ 61). Further, Patent Owner argues that the "on-chip" embodiment does not include a connection pin to provide a signal indicative of the DRAM temperature to an external circuit because, in response to the temperature, it generates internally a refresh pulse, which does not provide meaningful data based on the temperature sensor by a pin to an external circuitry. *Id*. (citing Ex. 1010, Fig. 8, 22:38–23:1). Furthermore, Patent Owner argues that adding components to Atkinson's "on-chip" embodiment with its on-board components would have increased the price, size, and complexity of the unit. *Id*. at 39 (citing Bernstein ¶ 63). Additionally, Patent Owner argues that Broadwater is not related to memory, DRAM or refresh, and offers no tradeoffs or incentives for additional on-board circuitry or pins for which the solution is to

reduce or cutoff circuit activity (as opposed to increasing circuit activity). *Id*. at 39–40 (citing Ex. 1006, 5:18–32). According to Patent Owner, Broadwater is concerned with combatting thermal stress from operating temperatures during operation. *Id*. at 40 (citing Ex. 1006, 1:30–51, 4:66–5:1). In Patent Owner's words, "while Atkinson is on, Broadwater is off, and vice versa." *Id*. (citing Ex. 2008 ¶¶ 63–66). Patent Owner argues that Atkinson and Broadwater are directed to very different applications. In particular, Atkinson is directed to making power use more efficient in laptops during system sleep, whereas Broadwater is directed to protecting mission critical circuitry in high speed aircraft. *Id*. (citing Ex. 1010, 3:6–28; Ex. 1006, 1:25–31).

Moreover, Patent Owner argues that although both Atkinson and Broadwater are focused on power efficiency, they do so by reducing circuit activity, whereas the '057 patent reduces waste of energy by increasing circuit activity. *Id*. at 40–41. That is, Atkinson prevents waste of energy by dropping circuit activity from a default level when the temperature drops, and Broadwater prevents waste of energy by dropping circuit activity from a default level when the temperature increases. *Id*. at 41 (citing Ex. 1010, 13:11–18; Ex. 1005, 5:18–27). In contrast, Patent Owner stresses that the '057 patent prevents waste of energy and failure by increasing circuit activity from a default level when the temperature increases. *Id*. (citing Ex. 1001, 3:55–66; Ex. 2008 ¶¶ 69–70). Therefore, Patent Owner submits that both Atkinson and Broadwater disclose cutting the temperature of the circuits, whereas

the '057 patent teaches increasing the circuitry temperature most when it is at its hottest. *Id*. (citing Ex. 1006, 5:18–27; Ex. 1010, 13:11–18;, Ex. 1001, 2:34–36, 3:55–58; Ex. 2008 ¶ 71).

A further difference argued by Patent Owner is that Atkinson is active when the external circuit is not operational, whereas the '057 is active when the external circuit is operational. *Id*. (citing Ex. 1010, 3:6–28; Ex. 1001, 2:1–2, 2:64–67; Ex. 2008 ¶ 72). Likewise, Patent Owner argues that Broadwater teaches shutting down part of the circuit, whereas the '057 "patent teaches keeping its DRAM active and working, since shutting down any portion would amount to a total data loss of that portion." *Id*. (citing Ex. 1006, 1:25–45; Ex. 1001, 1:51–59; Ex. 2008 ¶ 73).

Petitioner counters that Atkinson and Broadwater are directed to the same field of endeavor. Reply 2 (citing Ex. 1018, 38:3–6). According to Petitioner, chiefly among the ample reasons why a person of ordinary skill in the art would add Broadwater's functionality of reducing thermal stress in chips to Atkinson's circuitry is to prevent the DRAM in Atkinson from "blowing up" thereby furthering Atkinson's purpose of ensuring reliable operation of the chip. *Id*. at 2–3. Petitioner contends that because nothing in the claims requires the external pin to be used as part of the refresh process, there is no basis in the claims to support Patent Owner's argument that a temperature pin cannot be added to Atkinson's system, which performs the refresh process in a sleep mode. *Id*. at 3–4, 8. In particular, Petitioner argues because Atkinson's chip is still functioning even when it is in

sleep mode, it is still subject to overheating. *Id*. at 4. Therefore, Petitioner submits that the ordinarily-skilled artisan would have good reason to add the overheat protection of Broadwater to Atkinson's circuitry during periods of sleep mode and in the wake state because the external pin is not limited to a particular state. *Id*.

We agree with Petitioner. First, we agree with Petitioner that Atkinson and Broadwater are within the same field of endeavor because both references are generally within the field of integrated circuits. Reply 2. In particular, the references relate to optimizing the performance of integrated circuits by preventing the overheating thereof thereby enhancing reliability, temperature, and power consumption of integrated circuits. Further, Patent Owner's arguments regarding Atkinson are not commensurate in scope with the claim language. Patent Owner has not provided any basis in the claims to support the argument that Atkinson's system cannot be modified as proposed to add an external connection pin to complement the refresh process. The claim recitation "one connection pin such that the signal may be provided to external circuitry" implies that the external pin may be used as a vehicle for indicating the temperature of the DRAM to the external circuitry. However, as persuasively argued by Petitioner, the cited claim limitation does not restrict the use of the external pin/circuit to a particular state. Nor does it tie the external pin to the refresh process triggered in response to being informed of the DRAM temperature. As correctly noted by Petitioner, so long as Atkinson's DRAM is subject to disrupted

operation due to possible overheating (in the sleeping mode or wake state) and includes a temperature sensor that outputs the sensed temperature of the DRAM, its proposed combination with Broadwater would be proper because Broadwater's thermal stress reduction technique would help cool down the chip notwithstanding that the systems of Atkinson and Broadwater operate at different states. *Id*. at 4–5, 10. Accordingly, we agree with Petitioner that the teachings of Atkinson and Broadwater do not discourage the proposed combination.

ii. Whether Even If Atkinson and Broadwater Were Not Contrary to The Patent's Teaching, There Is No Reason to Combine Them to Make the Specific Invention Claimed.

Patent Owner argues that there is no reason to modify Atkinson to provide signals indicative of the onboard array temperature from the DRAM array to an external circuitry using Broadwater's external pin. PO Resp. 42 (citing Ex. 2008 ¶ 75). According to Patent Owner, adding an external pin to an existing DRAM is a very expensive and complex endeavor that counters the intended operation of Atkinson's self-refresh chip. *Id*. Patent Owner contends that because Atkinson's system performs an internal refresh operation in the sleep mode, the additional expense and complexity associated with adding an external pin would not be justified. *Id*. at 43–44. Moreover, Patent Owner contends that adding a forward biased diode as the temperature sensor would further increase the energy drain "sleep" mode. *Id*. at 44 (citing Ex. 2008 ¶¶ 78–79). Additionally, Patent Owner argues that neither

Atkinson nor Broadwater discloses any teachings pertaining to external control of DRAM timing to facilitate efficient, deterministic control of the DRAM in sync with the rest of the activity of the system. *Id*. at 45–46 (citing Ex. 2008 ¶ 82).

These arguments are not persuasive. As correctly noted by Petitioner, because the claims do not recite any limitation regarding external control of DRAM timing, Patent Owner's arguments are misplaced and are not commensurate with the scope of the claims. Reply 8. Further, we agree with Petitioner that adding a pin to Atkinson's chip for the purpose of communicating the sensed temperature of the DRAM to the external circuit, as taught by Broadwater, was well within the purview of the ordinarily-skilled artisan. *Id*. at 6–7, 9–10. As acknowledged by Patent Owner, Broadwater's disclosed technique pertains to a refresh circuit producing a refresh signal to reduce thermal stress in an integrated circuit (e.g., Atkinson's DRAM) in response to receiving from an external pin a signal indicating thermal distress in the chip. PO Resp. 36 (citing Ex. 1006, 2:31–38). Thus, we agree with Petitioner that because Broadwater's teachings pertain to relieving any type of chips from thermal distress, the ordinarily-skilled artisan would have been apprised that such a communication of the sensed temperature of the DRAM to the external circuitry via the external pin is a suitable addition to complement Atkinson's refreshing circuit in relieving the DRAM from possible overheating. Pet. 31 (citing Ex. 1005 ¶¶ 85, 86); Reply 7–8. Accordingly, we agree with Petitioner that there are sufficient reasons to combine the teachings of Atkinson and

Broadwater to yield the specific invention claimed. Reply 3–4.

iii. Whether the Proposed Atkinson-Broadwater Combination Would Require Extensive Modifications of Atkinson to Practice the Claims.

Patent Owner asserts that "a combination of Atkinson and Broadwater to practice the claims would require extensive modifications." PO Resp. 48. Specifically, Patent Owner argues that the proposed modification of Atkinson to add a connection pin would be extensive. *Id.* In particular, Patent Owner argues that such modification would require (1) selecting Atkinson's non-preferred embodiment with an on-chip temperature sensor in direct communication with the DRAM; (2) removing the temperature-sensing refresh generator from main memory so as to justify providing the signal to external circuitry; (3) adding a connection pin to the on-chip DRAM module; (4) generating a signal indicative of temperature that may be provided over the pin; (5) having the external circuitry in active mode while its energy saving system is working (not in sleep mode); (6) adding logic permitting DRAM to be refreshed at higher than default operation rate in high temperature situations; and (7) replacing temperature sensor with forward-biased diode. *Id.* at 48–50 (citing Ex. 2008 ¶¶ 85–91).

These arguments are not persuasive. We agree with Petitioner that none of these arguments has any basis in the claims. Reply 9. Further, we do not find any support on this record that Petitioner's proposed combination of Atkinson and Broadwater would require the cited modifications above, as

alleged by Patent Owner in reliance upon Dr. Bernstein's Declaration. The alleged modifications are incorrectly premised upon the substitution of Atkinson's onboard refresh unit with Broadwater's external refresh unit. Instead, the modification proposed by Petitioner contemplates adding a pin to Atkinson's on-board circuit to communicate the sensed temperature of the DRAM to the external circuit. Pet. 17 (citing Ex. 1005 ¶¶ 47–49); *id*. at 30 (citing Ex. 1006, 4:31–33, 4:49–53; Ex. 1005 ¶¶ 83–84). Consequently, the resulting Atkinson-Broadwater system would offer the dual benefit of maximizing power saving during self-refresh timing sequence, as well as reducing thermal stress on the DRAM. *Id*. at 31 (citing Ex. 1006, 1:14–29; Ex. 1005 ¶¶ 85–86). Therefore, we agree with Petitioner that none of these arguments changes the conclusion that the proposed modification of Atkinson with Broadwater would reinforce Atkinson's onboard refresh unit thereby allowing Atkinson's system to combat both thermal distress and preserve energy consumption. Reply 2–3 (citing Ex. 1018, 38:3–6, 40:5–15, 20–25). Furthermore, we agree with Petitioner that because the laptop disclosed in Atkinson is vulnerable to overheating even in sleep mode, it could benefit from Broadwater's external refresh unit, which is designed to relieve such circuit from thermal distress irrespective that the latter external unit operates in the active mode. *Id*. at 10. Moreover, we agree with Petitioner because Atkinson discloses a system configured to increase or decrease the DRAM refresh rate proportionally with the sensed temperature of the DRAM, a person of ordinary skill in the art (POSITA) would have been motivated to supplement Atkinson's circuitry with

Broadwater's external refreshing circuit as a way to keep the DRAM operating at all times. *Id.* at 10–11. On this record, we are not persuaded that the proposed Atkinson-Broadwater combination would require extensive modifications of Atkinson to practice the claims.

iv. Whether Petitioner and Its Declarant Wave Aside the References' Disclosures and Rely on Generalities and Offhand Comments in Each Reference

Patent Owner alleges that both Petitioner and its declarant rely on virtual irrelevancies, instead of main teachings from the references, in an attempt to show a motivation to combine the references. PO Resp. 51. In particular, Patent Owner offers the following examples of alleged generic Petitioner's statements: "it is desirable for the computer or external circuitry to be aware of the temperature for thermal management reasons," "to 'monitor and track the memory temperature for diagnostic purposes,'" "to enable throttling of power to reduce heat." *Id.* According to Patent Owner, such statements are conclusory and "would apply to anything that uses temperature as an input." *Id.* Further, Patent Owner argues that "Petitioner's declarant, at deposition, ignored or waved away most of the disclosures of both references in order to dwell on minute offhand comments in both references that he argued lend purported support to the combination." *Id.* at 52. In particular, Patent Owner argues that Petitioner's declarant, Dr. Subramanian, "dwelled [at his deposition] on Broadwater's asides" such as concepts that might be useful at low temperatures (*id.* (citing Ex. 2009,

147:24–148:21, 160:16–165:2)); whereas "Broadwater is directed to alleviating thermal stress from overheating circuitry by selectively shutting off parts of the overheated circuitry to reduce its temperature." *Id*. (citing Ex. 1006 1:14–45, 3:48–64, 5:35–45). Likewise, Patent Owner argues that "Atkinson is wholly directed to DRAM low-temperature self-refresh in non-operation;" whereas declarant's deposition "dwelled" on the comment that in Atkinson "'the refresh rate may be varied according to temperature during normal computer operation.'" *Id*. at 52–53 (citing Ex. 1010, 6:5–8; Ex. 2009, 175:12–176:10, 182:14–24). Patent Owner, therefore, submits that none of these off-hand comments corresponds to any explicit embodiments or substantial teachings in the references about how the completed applications might be accomplished. *Id*. at 53 (citing Ex. 2008 ¶¶ 95–98).

These arguments are not persuasive. We agree with Petitioner that the asserted motivation statements are not generalities, but pertain to reasons why a POSITA would have combined the teachings of Atkinson with Broadwater's. Reply 12. In particular, we agree with Petitioner that, as taught in Broadwater, thermal stress reduction during the operation of integrated chips has been recognized in the semiconductor art as a significant problem to be addressed. *Id*. (citing Pet. 30; Ex. 1006, 1:14–22). Likewise, we agree with Petitioner that even Patent Owner's expert acknowledges the benefit of preventing ICs from "blowing up." *Id*. at 13 (citing Ex. 1018, 40:12–15, 141:7–12).

On the record before us, we are persuaded that there is adequate motivation to modify Atkinson's

sensor to add Broadwater's connection pin so as to provide a signal indicative of the DRAM sensed temperature to an external circuitry for the purpose of reducing thermal stress in Atkinson's integrated circuit.

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater.

b. The Allegation That "Petitioner Has Failed to Show it Was Obvious to Modify Atkinson to Add the 'Diode' Limitations" (claims 2, 4, 10, 11, 14, 15, and 17)

Dependent claims 2, 4, 10, 11, 14, 15, and 17 recite, in relevant part, "wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode." Ex. 1001, 6:8–12.

1. Petitioner's Positions

Petitioner contends claims 2, 4, 10, 11, 14, 15, and 17 are unpatentable under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson, Broadwater, and Miller.[7] Pet. 20–21, 22, 25, 27, 28,

[7] Although Miller is omitted from the Petition's summary of asserted grounds, it was nevertheless relied upon in Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17. *See, e.g.*, Pet. 20. We, therefore, in the Decision on Institution treated Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and

29–30. Relying on the declaration of Dr. Subramanian, Petitioner explains how the proposed combination of references discloses all of the claim limitations. *Id.* (citing Ex. 1005). In particular, Petitioner asserts that, although the '057 patent includes a diode as a known temperature sensor, it also discloses other known temperature sensors (e.g., thermocouples, thermistors, or any other device that provides an output signal varying as a function of temperature). Pet. 20 (citing Ex. 1001, 2:42–45). Petitioner further asserts that Atkinson similarly discloses the use of such known temperature sensors (e.g., thermocouple or temperature sensing integrated circuit). *Id.* (citing Ex. 1010, 22:21–24; Ex. 1005 ¶¶ 52, 53). Petitioner then contends that, at the time of the invention, measuring a forward voltage drop across a semiconductor diode to thereby read the temperature, as described in Miller, was a well-known use of such a type of temperature sensor. Pet. 20 (citing Ex. 1015, Abstract). Petitioner concludes it would have been obvious to one of ordinary skill in the art to select a diode as a well-known type of temperature sensor for reading the temperature of Atkinson's DRAM. *Id.* at 21 (citing Ex. 1010, 24:63–65; 1005 ¶ 53). We are persuaded by Petitioner's showing and find that Miller's description of a diode as a temperature sensor would complement the Atkinson-Broadwater combination to teach using the diode to sense the temperature of the DRAM, which is communicated to an external circuitry via an external pin.

Likewise, claim 4 depends directly from claim 1,

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17 based upon Atkinson, Broadwater, and Miller as a separate ground of unpatentability. Inst. Dec. 5.

and recites

> wherein the at least one temperature sensor includes a diode having a forward voltage drop that varies as a function of the temperature of the DRAM array; the at least one connection pin includes a first pin coupled to an anode of the diode and a second pin coupled to a cathode of the diode; and the signal corresponds to a potential voltage between the first and second pins.

Ex. 1001, 6:17–23. Petitioner explains, with supporting evidence, that at the time of the invention, "given that the claim merely recites 'first pin' and 'second pin,' the diode temperature sensor would necessarily be connected to a first pin and a second pin if it were operational." Pet. 22 (citing Ex. 1005 ¶ 56). Petitioner further explains that "in such a diode configuration, the signal between the first pin and the second pin would necessarily be the forward voltage drop of the diode, which claim 4 defines as the signal." *Id*. Petitioner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to "modify Atkinson to use a diode configuration as recited in claim 4 (which is essentially the same as the obvious variant in claim 2)." *Id*. We are persuaded by Petitioner's showing and find that Miller's diode coupled to the pins in Atkinson's DRAM teaches a forward biased diode connected to the connection pins.

We also have reviewed the Petition with respect to dependent claims 10, 11, 14, 15, and 17, and determine that Petitioner has accounted sufficiently

for the recited limitations. Pet. 25, 27, 28.

2. Patent Owner's Assertions Regarding the References

Patent Owner makes two principal arguments: (i) Miller was not part of any of the combinations expressly raised by the Petition (PO Resp. 19–28), and that (ii) Petitioner fails to show it was obvious to modify Atkinson to add the diode limitations. *Id*. at 53–57. We address each argument in turn.

i. The Allegation that Miller was not Part of Any Combination Expressly Raised in the Petition

Patent Owner argues that Petitioner did not expressly raise Miller as part of any of the combinations argued in the Petition. PO Resp. 54. In particular, Patent Owner argues that the Petition's "Summary of Grounds of Rejection" lists Atkinson and Broadwater as a possible combination, but never mentions Miller. *Id*. at 20. According to Patent Owner, while the Petition recognizes that the Atkinson-Broadwater combination is silent about the forward biased diode, it asserts that the ordinarily-skilled artisan would have known that forward biased diodes were well-known in the art for sensing temperature, and then lists Miller as an example of such common use of forward biased diode. *Id*. According to Patent Owner, such a reference to Miller in the Petition is not tantamount to including Miller as part of the Atkinson-Broadwater combination. *Id*. at 21. Patent Owner argues that the Board, sua sponte, redrafted the ground of unpatentability proposed by Petitioner to yield the Atkinson, Broadwater, and Miller combination as a separate and new ground in the Institution Decision

thereby converting Miller from background art to a reference in the combination. *Id.* at 19, 21–22. Consequently, Patent Owner submits that by instituting on the new ground combination, the Board has caused the following:

> (1) Deprived Patent Owner of its due process right to file a preliminary response as to the new ground (PO Resp. 23–24);
>
> (2) Violated the Board's regulations whereby the Petition must identify the challenge along with the specific ground (*id.* at 24–25);
>
> (3) Contradicted without reason Petitioner's choice of making Miller background art, as opposed to making Miller part of the combination (*id.* at 25);
>
> (4) Prejudiced Patent Owner by forcing it to consider and address the issue in its Patent Owner's Response (*id.* at 26); and
>
> (5) Contravened the Administrative Procedure Act's requirement to maintain an impartial stance by weighing on Petitioner's side of the controversy (*id.* at 26–28).

In response, Petitioner argues that Miller is introduced in Ground 1 of the Petition to teach using a diode detecting temperature in an integrated circuit. Reply 15 (citing Pet. 19–20). According to Petitioner, because Ground 2 builds off Ground 1, the Board properly interpreted Petitioner's intent to make Ground 2 additive to Ground 1, and therefore to include Miller, and that the heading or title within the Petition does not alter the underlying content of the Petition. *Id.* at 14–15.

We agree with Petitioner. As noted in the Institution Decision, Petitioner's discussion of Miller within the content of the Petition as a way to bolster the Atkinson-Broadwater combination is tantamount to the Atkinson-Broadwater-Miller combination. Inst. Dec. 5; Pet. 20–21. Patent Owner was apprised of the Petitioner's reliance on Miller in the Petition, and Patent Owner availed itself of the opportunity to provide arguments addressing Miller in the Patent Owner Response (see PO Resp. 53–57). Accordingly, we are not persuaded that the combination of Atkinson, Broadwater, and Miller was not raised in the Petition.

ii. The Allegation that There is No Motivation to Combine Miller with Atkinson

Patent Owner argues that because Miller does not discuss memory, DRAM, or DRAM refresh, substituting Miller's forward-voltage-drop diode for Atkinson's thermistor would not have been obvious to the ordinarily-skilled artisan. PO Resp. 54. According to Patent Owner, neither the Petitioner nor its declarant identifies a rationale supporting the proposed substitution of Atkinson's temperature sensors for Miller's diode. *Id*. at 55. Patent Owner further argues that merely indicating Miller's diode could be selected over the alternatives listed in Atkinson does not identify a rationale for the proposed substitution. *Id*. (citing Ex. 2008 ¶¶ 99–101). Furthermore, Patent Owner argues that because the claimed diode voltage sensor only works with the diode forward biased, the steady state current flowing through a voltage drop for sensing the temperature through the forward-biased diode would increase the steady state power during the

sleep mode. *Id*. Accordingly, Patent Owner submits that a diode would increase the sleep mode current drain, and would thereby violate Atkinson's desired reduction in energy consumption. *Id*. Additionally, Patent Owner argues that even if Miller were used as merely background information as intended by Petitioner, the Petition still fails to show that it would have been obvious to replace a generally known diode in place of Atkinson's thermistor because the limitation in question is not "'unusually' insignificant" and the technology "'particularly straightforward.'" *Id*. at 56. Patent Owner, therefore, submits that because the diode limitations are important structural limitations in the claim, replacing Atkinson's thermistor with Miller's generally known diode would change the operation of the device and necessitates modification of Atkinson's refresh generator. *Id*. at 57.

Petitioner counters that because diodes have been used for sensing temperature in integrated circuits since the 1970s, POSITA would have known that the proposed substitution is reasonable as conceded by Patent Owner's expert. Reply 13–14 (citing Ex. 1010, 22:21–26; Ex. 2009, 209:12–17; Ex. 1015; Ex. 1018, 188:19–25), 18–19. In particular, Petitioner argues that Broadwater's express teaching of using a diode to detect temperature (Ex. 1006, 3:55–58), taken in combination with Patent Owner's admission that a thermocouple is much like a forward biased diode (Ex. 1018, 180:6–10) supports the proposed combination. *Id*. at 14. Further, Petitioner submits that "[o]ne of ordinary skill in the art would be motivated to send the signal indicative of memory temperature to an external connection

pin, at least to enable its use in a cooling regime, such as the one set forth in Miller." Pet. 18. Additionally, Petitioner submits "[t]hose of ordinary skill at the time of the filing of the '057 [p]atent would know that one example of the finite alternate types of integrated circuits for detecting temperature was a diode having a forward voltage drop that varies as a function of temperature." *Id*. at 20.

We agree with Petitioner. As correctly argued by Petitioner, Patent Owner does not dispute that, at the time of the invention, using a diode for sensing the temperature of an integrated device was well-known in the art. Therefore, we agree with Petitioner that although Miller is not related to a memory type circuit, the forward-biased diode disclosed in Miller is directed to sensing integrated circuits as a whole including memory integrated circuits such as the DRAM disclosed in Atkinson. Reply 15–17. Further, as correctly noted by Petitioner, Atkinson, in fact, suggests using alternative temperature sensing devices not particularly listed for sensing the temperature of the DRAM. Pet. 20 (citing 1010, 22:21–24). Furthermore, we do not agree with Patent Owner that Petitioner has not provided sufficient motivation for substituting Miller's forward biased diode with Atkinson's thermistor. As noted above, Petitioner expressly asserts that the ordinarily-skilled artisan would have made the proposed substitution to enable the use of Atkinson's DRAM in a "cooling regime," as well as "to enable throttling of power to reduce heat as well as to monitor and track the memory temperature for diagnostic purposes." Pet. 18. Moreover, as discussed above, irrespective of

differing modes of Atkinson's DRAM, Broadwater's external circuit or Miller's forward biased diode, the overall combination of the cited references would predictably result in reducing thermal stress in the DRAM, upon being notified that the DRAM is overheating, thereby reducing the overall power consumption of the circuit. In other words, Petitioner's proposed combination of the cited teachings of Atkinson, Broadwater, and Miller is no more than a simple arrangement of old elements with each performing the same function it had been known to perform, yielding no more than one would expect from such an arrangement. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). The ordinarily-skilled artisan, being "a person of ordinary creativity, not an automaton," would be able to fit the teachings of the cited references together like pieces of a puzzle to predictably result in an external circuit that provides a proportional cooling signal to a DRAM circuit upon receiving a signal from a forward biased diode indicating a sensed temperature of the DRAM. *Id.* at 420–21. We are not persuaded that the Petitioner's proffered combination would have been "uniquely challenging or difficult for one of ordinary skill in the art"; we agree with the Petitioner that the proposed modification would have been within the purview of the ordinarily skilled artisan. *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 418).

Petitioner has sufficiently shown that it would have been obvious to use the diode described in Miller to read and measure the temperature of Atkinson's DRAM. Pet. 20–21. On the record before

us, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness based on Atkinson, Broadwater, and Miller. *See KSR*, 550 U.S. at 418.

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson, Broadwater, and Miller.

c. The Allegation that Petitioner Has Failed to Point Out Where the "Refresh Unit" (Claims 6–11) and the "Refresh Timing Unit" (Claims 7–11) Limitations Are Found.

Dependent claims 6–11 recite, in relevant part, "a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal." Ex. 1001, 6:28–30. Further, dependent claims 7–11 recite a "refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases." *Id*. at 6:36–39.

1. Petitioner's Positions

Petitioner asserts Atkinson describes a temperature sensing refresh generator that senses the main memory temperature to issue a refresh frequency that increases or decreases in proportion with the sensed temperature. Pet. 23 (citing Ex. 1010, 24:15–23; Ex. 1005 ¶ 58). Further, Petitioner asserts that Atkinson discloses an alternative embodiment with a voltage controller oscillator (VCO) combined with a temperature sensor,

whereupon the VCO receives from the sensor a sensed temperature signal of the main memory, the VCO, produces in response a proportional refresh signal to refresh the main memory. *Id.* (citing Ex. 1010, 23:8–10, 23:17–20). We are persuaded by Petitioner's showing and find that Atkinson's description of the refresh generator teaches a refresh unit for providing to the DRAM an increased or decreased refresh rate in proportion with the sensed temperature of the DRAM. Likewise, we are persuaded that Atkinson's description of the VCO teaches a refresh timing unit to decrease the rate at which the DRAM array is refreshed as the signal indicates the temperature of the DRAM decreases.

2. Patent Owner's Assertions Regarding the References

As to the terms "refresh unit" and "refresh timing unit" recited in claims 6–11, Patent Owner argues the following:

> (i) Petitioner fails to show that Atkinson teaches "'a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal'" (PO Resp. 58–59), and that
>
> (ii) Petitioner fails to show Atkinson teaches "'a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal.'" *Id.* at 59–60.
>
> We address each argument in turn.

i. The Allegation that Petitioner Fails to Show that Atkinson Teaches "a Refresh Unit Operable to

Refresh the DRAM Array at a Rate that Varies in Response to the Signal"

Patent Owner argues that the statement in Atkinson relied upon by Petitioner teaches, at most, that the rate and the temperature are linked, but not that the rate "'varies in response to the signal.'" PO Resp. 58 (quoting Ex. 101, 24:15–23). According to Petitioner, the signal described in the statement is not equivalent to the signal recited in claim 6 because the signal described in Atkinson relates to a periodic voltage pulse produced by Atkinson's generator, whereas the claimed signal relates to a signal produced by the temperature sensor. *Id*. at 58–59. Accordingly, Patent Owner submits that Atkinson does not teach the required limitation of a signal indicative of the temperature of the DRAM array. *Id*. at 59.

This argument is not persuasive for the same reasons previously noted in our institution Decision. In particular, we noted the following:

> The antecedent basis for "the signal" is in claim 1, where Petitioner relies upon Atkinson's teaching of the refresh generator output, which is indicative of the temperature of the DRAM as measured by thermistor 800. Pet. 14–17 (discussing embodiments described in Figures 8 and 9 of Atkinson). In connection with the embodiment of Figure 8, Atkinson teaches explicitly that "[t]he frequency of the refresh signal in this embodiment continuously reduces as temperature decreases, rather than in discrete steps as in prior

> embodiments. Thus, refresh generator 850 provides a refresh signal that closely follows the temperature/frequency response of curve 600 or any other desired temperature/frequency response curve." Ex. 1010, 22:62–23:1. As a result, we agree with and are persuaded by Petitioner's contentions that Atkinson teaches refreshing the DRAM array at a rate that varies in response to the signal, as claim 6 requires, and not merely in response to the temperature of the DRAM array, as Patent Owner suggests.

Inst. Dec. 15–16.

We, therefore, reiterate our agreement with Petitioner that because Atkinson's refresh unit generates the refresh signal in response to receiving the DRAM temperature signal such that the generated refresh signal track the temperature signal proportionally, the generated refresh signal teaches the temperature signal. Reply 19–20.

On this record, Petitioner has shown by a preponderance of the evidence that Atkinson teaches "a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal."

ii. The Allegation that Petitioner Fails to Show Atkinson Teaches "'a Refresh Timing Unit Operable to Establish the Rate at Which the DRAM Array is Refreshed in Response to the Signal'"

Patent Owner argues Petitioner does not show that Atkinson's VCO is operable to establish the rate at which the DRAM array is refreshed in response to the sensed temperature signal. PO Resp. 59–60.

According to Patent Owner, Atkinson's VCO merely 'produces a periodic waveform having a frequency that changes in response to changes in the input voltage. *Id*. at 60 (quoting Ex.1010, 23:5–9).

This argument is not persuasive. We agree with Petitioner that because Atkinson's VCO "'produces the refresh signal at the proper frequency'" in response to receiving a signal indicative of the temperature, the generated refresh signal sets the frequency to refresh the DRAM. Reply 21.

On this record, Petitioner has shown by a preponderance of the evidence that Atkinson teaches "'a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal.'"

d. Weight to be Given to Dr. Subramanian's Declaration

Patent Owner argues that no weight should be given to Dr. Subramanian's declaration because the declarant is not an attorney, he applied an incorrect legal test, and he is thereby not suited to provide opinions on the legal question of obviousness. PO Resp. 28–29. In support of this argument, Patent Owner directs attention to portions of Dr. Subramanian's deposition where he allegedly testified that background knowledge (including common sense) of an ordinary artisan can be routinely added to a combination to teach a missing limitation, even if the missing limitation "'went to the heart of the invention.'" *Id*. at 29. According to Patent Owner, because the legal test allegedly applied by Dr. Subramanian was previously rejected by the Board's reviewing court in *Arendi S.A.R.L. v.*

Apple Inc., 832 F.3d 1355, 1361–65 (Fed. Cir. 2016) (2), the Board should disregard Dr. Subramanian's opinions on the ultimate question of obviousness. *Id.* at 29–30. Further, Patent Owner argues that Petitioner's declaration should be given little to no weight because the declaration allegedly parrots Petitioner's attorney's arguments. *Id.* at 30–31. According to Patent Owner, Petitioner's declaration section VII-B, for example, is exactly the same as Petition's section VII-B. *Id.* (citing Pet. 29–32; Ex. 1005, 28–30).

We have reviewed the arguments provided by Patent Owner and determine such arguments are insufficient to have Dr. Subramanian's declaration disregarded in its entirety. Rather, it is within our discretion to assign the appropriate weight to be accorded evidence. *See* 37 C.F.R. § 42.65(a); *see also, e.g., Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its] discretion."). Based on the record before us, we are not persuaded that we should give the entirety of Dr. Subramanian's declaration no weight. We reiterate nonetheless that we reached the ultimate conclusion of obviousness in this

Decision based on the totality of the record before us, and without adopting any purported "lay opinions".[8]

e. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence the following:

(1) Claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater;

(2) Claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson, Broadwater, and Miller.

III. CONCLUSION

Petitioner has demonstrated, by a preponderance of the evidence, that:

(1) Claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater;

(2) Claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson, Broadwater, and Miller.

IV. ORDER

Accordingly, it is

ORDERED that claims 1–17 of the '057 patent are determined to be *unpatentable*;

FURTHER ORDERED that, because this is a

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[8] See supra note 5.

Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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APPENDIX F

Trials@uspto.gov Paper 9
571-272-7822 Entered: March 29, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE
PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,
v.
POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2017-00116
Patent 7,334,150 B2

Before SALLY C. MEDLEY, BARBARA A. PARVIS, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–3, 5, 6, and 8–11 of U.S. Patent No. 7,334,150 B2 (Ex. 1001, "the '150 Patent"). Paper 2 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); see 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude Petitioner demonstrates a reasonable likelihood of prevailing in demonstrating the unpatentability of the challenged claims of the '150 Patent and, therefore, we institute an *inter partes* review as to these claims on the grounds specified below.

A. Related Matters

The parties state that the '150 Patent is the subject of a pending lawsuit in the Central District of California, i.e., Polaris Innovations Ltd. v. Kingston Tech. Co., Case No. 8:16–cv-300 (C.D. Cal.)[1] and the lawsuit includes assertions against Petitioner. Pet. 2; Paper 3 (Patent Owner's Mandatory Notices), 1.

B. The '150 Patent

The '150 Patent is directed to a semiconductor

[1] This lawsuit is referred to herein as the "companion district court lawsuit."

memory module that includes a register circuit and a clock signal regeneration circuit. Ex. 1001, 1:9–16. Figure 2 is reproduced below.

FIG 2

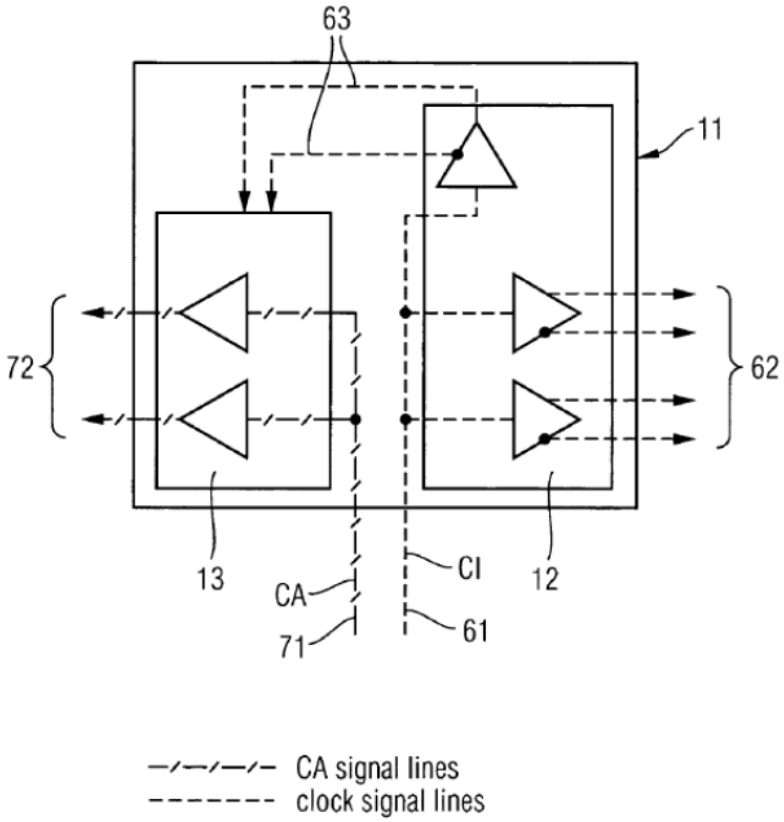

Figure 2 shows a top view of a clock signal regeneration circuit and register circuit in a common chip packing.

As shown in Figure 2 above, chip packing 11 contains clock signal regeneration circuit 12 and

register circuit 13. Ex. 1001, 4:30–33. Differential clock signal input line 61 supplies clock signal Cl to common chip packing 11. *Id*. at 4:41–43. Line section 71 supplies command and address input signals "CA." *Id*. at 4:43–45. Differential clock signal lines 62 from clock signal regeneration circuit 12 supply the conditioned clock signal to memory chips 4 and 4*a*. *Id*. at 4:49–53. Differential clock signal lines 63 supply the conditioned clock signal to register circuit 13. *Id*. at 4:54–56. From register circuit 13, temporarily stored command and address signals are supplied by differential command and address signal lines 72 to memory chips 4 and 4*a*. *Id*. at 4:56–60.

C. Illustrative Claim

Petitioner challenges claims 1–3, 5, 6, and 8–11 of the '150 Patent. Claim 1 is an independent claim. Claims 2, 3, 5, 6, and 8–11 depend directly from claim 1. Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A memory module comprising:
>
> a plurality of memory chips arranged on the memory module;
>
> a plurality of bus signal lines operable to supply an incoming clock signal and incoming command and address signals to at least the memory chips;
>
> a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to supply the copies of the incoming clock signal to the memory chips, the copies of the incoming clock signal having a same frequency as the

incoming clock signal; and

a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit, the register circuit being further configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a same frequency as the incoming command and address signals.

Id. at 7:1–25.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–3, 5, 6, and 8–11 are unpatentable based on the following grounds (Pet. 4):

Reference(s)	**Basis**	**Challenged Claim(s)**
Dodd[2]	§ 103(a)	1, 2, 5, 6, and 8–10
Dodd and Keeth[3]	§ 103(a)	3 and 11
Lee[4]	§ 103(a)	1, 2, 5, 6, and 8–

[2] U.S. Patent No. 6,530,006 B1, issued Mar. 4, 2003 (Ex. 1003) ("Dodd").
[3] U.S. Patent No. 7,123,046 B2, issue Oct. 17, 2006 (Ex. 1016) ("Keeth").

		10
Lee and Keeth	§ 103(a)	3 and 11

As support, Petitioner proffers a Declaration of Dr. Vivek Subramanian, who has been retained by Petitioner for the instant proceeding. Ex. 1011 ¶¶ 1–3.

II. DISCUSSION

A. Overview

A patent claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

B. Person of Ordinary Skill in the Art

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[4] U.S. Patent No. 6,898,726 B1, issued May 24, 2005 (Ex. 1008) ("Lee").

Petitioner proposes that a person of ordinary skill in the art had a Master's degree in Electrical Engineering and at least 2 years' experience working in the field of semiconductor memory design. Ex. 1003 ¶¶ 17–19 (cited e.g., in Pet. 7). Patent Owner does not dispute Petitioner's proposal. *See generally* Prelim. Resp. We adopt Petitioner's proposed definition for the purposes of this Decision.

We also consider the level of skill implied by the disclosures of the prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of skill in the art). Additionally, this person is of ordinary creativity, not an automaton. *KSR*, 550 U.S. at 421.

C. Claim Construction

Petitioner provides proposed constructions for certain terms, set forth below (Pet. 12–17).

Term	Petitioner's Proposed Construction
"memory module"	"[a] removable circuit board, cartridge, or other carrier that contains one or more memory chips."
"having a same frequency"	"with no intended modification from the frequency of the incoming signal."
"RDIMM"	"a Dual In-Line Memory Module that has circuitry to buffer control signals, addresses, or data."

Patent Owner makes two arguments in response: (1) Petitioner should be held to its previous arguments in the companion district court lawsuit (Prelim. Resp. 5–26, 31–32); and (2) certain of Petitioner's constructions interject vague terms, i.e., "removable" and "intended" (*id*. 27–31).

1. Whether Petitioner Should Be Held to Companion District Court Lawsuit Positions

We turn to Patent Owner's contention that Petitioner should be held to its previous arguments in the companion district court lawsuit. Prelim. Resp. 5–26, 31–32. Patent Owner, more specifically, points to Petitioner's alleged previous arguments in the companion district court lawsuit that (1) "clock signal regeneration circuit" and "a register . . . configured to . . . generate a plurality of copies of the incoming command and address signals" are means-plus-function limitations (*id*. at 5–16); (2) claim 6 is indefinite (*id*. at 16–26); and (3) "RDIMM" register circuitry buffers only command and address signals, not data (*id*. at 31–32).

Claims that include the language "means" or "means for" are presumed to invoke 35 U.S.C. § 112 ¶ 6.[5] *See Williamson v. Citrix Online, LLC*, Case No. 2013-1130, slip op. 16 (Fed. Cir. June 16, 2015) (en banc in relevant part) ("use of the word 'means' creates a presumption that § 112, ¶ 6 applies.").

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[5] Section 4(c) of the Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA") re-designated 35 U.S.C. § 112 ¶ 6, as 35 U.S.C. § 112(f). Because the '150 Patent has a filing date before September 16, 2012, the effective date of § 4(c) of the AIA, we will refer to the pre-AIA version of 35 U.S.C. § 112.

However, the terms "clock signal regeneration circuit" and "a register . . . configured to . . . generate a plurality of copies of the incoming command and address signals" do not contain the language "means" or "means for."

As Petitioner correctly contends (Pet. 11), and Patent Owner acknowledges (*see, e.g.*, Prelim. Resp. 10, 30) in an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). In the instant proceeding, neither party contends that the independent claims recite "means" or "means for," or contends that 35 U.S.C. § 112, ¶ 6 should apply to "clock signal regeneration circuit" or "a register . . . configured to . . . generate a plurality of copies of the incoming command and address signals." Pet. 11–16; Prelim. Resp. 5–16. Furthermore, Patent Owner has provided only partial evidence of the parties' claim construction contentions in the companion district court. Prelim. Resp. ix; Ex. 2002.

Based on the record before us at this juncture of the proceeding, we are not persuaded that either "clock signal regeneration circuit" or "a register . . . configured to . . . generate a plurality of copies of the incoming command and address signals" invokes § 112 ¶ 6. This determination is sufficient to resolve the only dispute between the parties at this juncture, which is whether Petitioner has satisfied 37 C.F.R. § 42.104(b)(3).

6 Accordingly, we determine that it is not necessary to provide an express interpretation of

"clock signal regeneration circuit" or "a register . . . configured to . . . generate a plurality of copies of the incoming command and address signals." *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("[C]laim terms need only be construed 'to the extent necessary to resolve the controversy'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Regarding Patent Owner's contention that Petitioner should be held to its previous arguments in the companion district court lawsuit that claim 6 is indefinite, in the instant proceeding, neither party contends that claim 6 is indefinite. *See, generally*, Pet.; Prelim. Resp. 16–26. Furthermore, Patent Owner again has provided only partial evidence of the parties' claim construction contentions in the companion district court lawsuit and has not submitted a decision in the companion district court lawsuit determining that claim 6 is indefinite. Prelim. Resp. ix; Exs. 2001, 2003. We determine that it is not necessary to provide an express interpretation of the term to resolve a dispute between the parties at this juncture of the proceeding.

We turn to Patent Owner's contention that Petitioner should be held to its previous arguments in the companion district court lawsuit that "RDIMM" register circuitry buffers only control and address signals, not data. Prelim. Resp. 31–32. Neither of the parties contends that this construction is appropriate in the instant case. Instead, Petitioner contends that "RDIMM" stands for registered dual in line memory module. Pet. 37. Patent Owner does not disagree and, further, does

not dispute that RDIMMs were known prior art devices. Prelim. Resp. 48.

Additionally, we need not limit "RDIMM" to register circuitry that buffers only control and address signals to address Patent Owner's asserted inconsistency with respect to Dr. Subramanian's testimony. *Id*. at 31 (citing Ex. 1011 ¶ 32). Dr. Subramanian testifies that "the BRI of the term 'RDIMM' is 'a DIMM that has register circuitry to buffer control signals.'" Ex. 1011 ¶ 32. Independent claim 1 recites that a "memory module, comprising" "a register circuit," and, claim 10, which depends directly from claim 1, further recites that the "memory module comprises an RDIMM module." Based on the record before us, including the aforementioned express recitations of the claims, at this juncture of the proceeding, we determine that it is not necessary to provide an express interpretation of the term "RDIMM" to resolve a dispute.

2. Whether Petitioner's Proposed Constructions Introduce Vague Terms

We now turn to Patent Owner's argument that certain of Petitioner's proposed constructions interject vague terms, i.e., "removable" and "intended" (Prelim. Resp. 27–31). Regarding "removable" in Petitioner's proposed construction of "memory module" (Pet. 12–13) recited in claim 1, Patent Owner does not dispute that the asserted prior art teaches a memory module. *See generally* Prelim. Resp. Additionally, Patent Owner specifically contends that "Patent Owner acquiesces" to Petitioner's proposal "for present purposes." *Id*. at 28. Accordingly, we determine no express

construction of the term "memory module" is needed to resolve a dispute between the parties based on the current record at this juncture.

With respect to "intended" within Petitioner's proposed construction for "same frequency" (Pet. 13–16) recited in claim 1, Petitioner's proposal is based on remarks made during prosecution (*id*. at 15–16). Petitioner contends (*id*. at 13) and Patent Owner does not dispute (Prelim. Resp. 28–31) that the phrase "having the same frequency" did not appear in the specification or claims as filed, but was added by amendment. Patent Owner's proposal is to remove the word "intended" from Petitioner's proposed construction. *Id*. at 30–31.

Although Patent Owner disputes that Lee teaches a copy of a clock having the same frequency (*id*. at 50), based on the record before us at this juncture, resolution of this dispute does not hinge on whether we adopt Patent Owner's proposal regarding the word "intended." Instead, the dispute pertains to whether the frequency may be adjusted. *See id*. at 51 ("[A] copy ***at half frequency***" is "not at 'a same frequency.'").

We begin by noting that "same frequency" is within a larger phrase, set forth below.

> To generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a *same frequency* as the incoming command and address signals.

Ex. 1001, 7:20–25.

Based on the record before us at this juncture, we decline to construe the full phrase above such that both the generated copies and the copies that are supplied are required to be at the same frequency as the incoming signals. Instead, we consider embodiments set forth in the '150 Patent Specification, including a preferred embodiment, in which intermediary frequency adjustments are made. For instance, in the Summary of the Invention, the '150 Patent describes that "CA signals are multiplied by a factor of 1:X" so that "several CA copies can be provided to several branches." Ex. 1001, 2:2:57–59; *see also id*. at 3:61–64 ("The register and clock signal regeneration circuits are, *preferably*, designed such that they each multiply the clock signal and the command and address signal by a factor of 1:2" (emphasis added)). Based on the current record before us at this juncture, we determine no other express construction of the term "same frequency" is needed to resolve a dispute between the parties based on the current record at this juncture.

D. Evidentiary Weight of Declaration Evidence

In addition to the asserted prior art, the Petition relies upon Dr. Subramanian's Declaration (Ex. 1011). Patent Owner contends that we should accord Dr. Subramanian's testimony no evidentiary weight because he "merely parrots the Petition." Prelim. Resp. 32–35. Patent Owner provides an exemplary comparison (*id*. at 33–34) and submits a table with additional comparisons (Ex. 2004).

Based on the record before us and at this juncture, we decline to disregard the Declaration (Ex.

1011) as Patent Owner suggests. We are not convinced that any similarities in the Petition and Dr. Subramanian's Declaration necessarily indicate that the Declaration is a copy of an attorney-prepared Petition. Instead, the Petition may be a copy of the Declaration or Dr. Subramanian may have worked with the attorneys to prepare both the Petition and Declaration simultaneously.

E. Obviousness of Claims over Dodd alone or with Keeth

Petitioner contends claims 1, 2, 5, 6, and 8–10 are unpatentable under 35 U.S.C. § 103(a) as obvious over Dodd.[6] Pet. 4, 18–39. Petitioner contends claims 3 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Dodd and Keeth. *Id.* at 4, 39–41.

1. Overview of Dodd

Dodd is directed to a buffered memory system with data buffers, an address/command buffer, and a clock circuit. Ex. 1003, Abstract. Figure 1 of Dodd is reproduced below.

[6] Although claim 11 is listed in the section heading for this ground (Pet. 18), the analysis of claim 11 is found within only the next section (*id.* at 39–41).

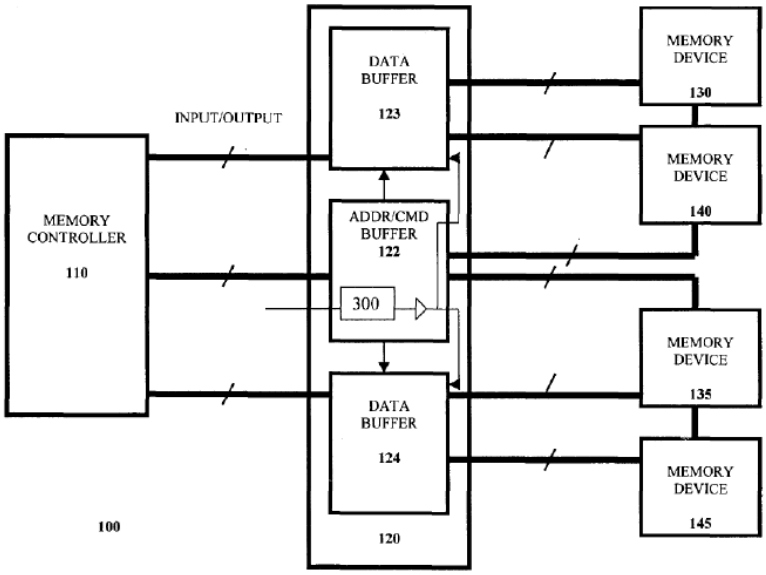

FIG. 1

Figure 1 illustrates a buffered memory system.

As shown in Figure 1 above, buffered memory system 100 comprises memory controller 110, buffer 120, and memory devices 130–145. *Id.* at 2:39–43. Memory controller 110 is connected to buffer 120, which is connected to memory devices 130–145 so that status, address, and command information, as well as data are transmitted from memory controller 110 to memory devices 130–145 via buffer 120. *Id.* at 2:56–61. Memory controller 110 also receives data from memory devices 130–145 via buffer 120. *Id.* at 2:61–63.

2. Overview of Keeth

Keeth is directed to adaptively adjusting a transition threshold of a data receiver using differential clock signals and a reference voltage. Ex.

1016, Abstract. According to Keeth, Double Data Rate Dynamic Random Access Memory (DDR DRAM) devices use differential signaling for clock signals at clock pins of a device package. *Id*. at 1:22–30. DDR DRAM devices use non-differential signaling for data signals input on the device data pins. *Id*. at 1:35–37.

3. Discussion of Claim 1

We begin our analysis with independent claim 1. Claim 1 is directed to a memory module comprising memory chips and bus lines. Ex. 1001, 7:1–7. Petitioner points to teachings relating to Dodd's memory module 150. Pet. 21–24 (citing Ex. 1003, 2:39–63, 3:51–4:14, 5:57–6:7, Figs. 1, 3, 5; Ex. 1011 ¶¶ 38–40). Consistent with Petitioner's contentions (*id*.), Dodd teaches a buffering structure, including data buffers 123 and 124, and an address and command buffer 122 that, in accordance with one embodiment, is housed within memory module 150 along with memory devices 1–8 (*see, e.g.*, Ex. 1003, 5:57–63, Fig. 5). The memory module includes bus lines for receiving data, address, and command signals as well as clock signals. Ex. 1003, 5:63–6:11, Figs. 1, 3, 5.

Claim 1 also recites a clock signal regeneration circuit configured to generate copies with the same frequency as the incoming clock signal and supply the copies to the memory chips. Ex. 1001, 7:8–13. Petitioner points to the clock circuit in the memory module that generates and supplies copies of the clock signal. Pet. 24–25 (citing Ex. 1003, 3:51–4:18, 5:6–32, 5:57–6:20, Figs. 3, 5; Ex. 1011 ¶¶ 41, 42). Consistent with Petitioner's contentions (*id*.), Dodd teaches clock circuit 300 that copies input clock 10

and drives output clock 20 to the data buffers 123 and 124 so that the memory devices receive the signals in one clock command. Ex. 1003, 3:67–4:18; see also id. at 5:57–6:20 (teaching implementing embedded clock signal 300 to synchronize clocking of data buffers 123 and 124 and memory devices 1 through 8 with that of address command buffer 122). Dodd also teaches implementing clock circuit 300 as a PLL such that "[w]hen the PLL is 'locked' the frequency and phase of the output signal are the same as those of the input signal." *Id.* at 5:6–32.

Claim 1 additionally recites a register circuit arranged on the memory module in a common chip packing with the clock regeneration circuit and configured to receive copies of the clock signal from the clock regeneration circuit. Ex. 1001, 7:14–18. Petitioner points to Dodd's teachings relating to the buffering structure, for example, buffer 120. Pet. 25–28 (citing Ex. 1003, 2:1–5, 2:39–3:12, 3:51–4:18, 5:5–25, 5:57–6:11, Figs. 1, 3–5; Ex. 1011 ¶¶ 19, 43–46). Consistent with Petitioner's contentions (*id.*), Dodd, for example, teaches "buffer 120 is an external buffer(s) or register(s)" (Ex. 1003, 2:43–45), which has "embedded therein a clock circuit 300 and a clock driver 310" (*id.* at 6:1–3). Additionally, Dodd teaches an embodiment in which clock circuit 300 is embedded within address and command buffer 122 and copies of the clock signal are received by data buffers 123 and 124, all within buffer 120. *Id.* at 5:57–6:11, Fig. 5. In accordance with this embodiment, Dodd further teaches that the buffering structure includes address and command buffer 122, embedded clock circuit 300, and data buffers 123 and 124, and that this buffering structure and memories

1–8 are within memory module 150. *Id*.

Claim 1 further recites that the register circuit is configured to temporarily store and then supply to the memory chips copies of command and address signals having the same frequency as the incoming command and address signals. Ex. 1001, 7:18–25. Petitioner references back to other portions of the Petition discussed above, as well as to teachings relating to the buffering structure and, more specifically, address and command buffer 122 therein. Pet. 28–31 (citing *e.g.*, Ex. 1003, 2:39–3:12, 3:51–4:18, 5:60–65, Figs. 1, 3, 5; Ex. 1011 ¶¶ 47–52). Relying on the testimony of Dr. Subramanian, Petitioner also contends that an ordinarily skilled artisan would have recognized that Dodd's buffering structure does not change the frequency of the buffered signals. Pet. 31 (citing Ex. 1011 ¶ 52). Consistent with Petitioner's contentions, Dodd teaches "a buffered memory" including "ADDR/CMD buffer 122" (Ex. 1003, 5:57–61) and that "information such as data, status information, address information and command information" are transmitted "to the memory devices 1–8 via the buffering structure" (*id*. at 5:63–66).

We turn now to Patent Owner's contentions. Our claim construction discussion above addresses Patent Owner's contentions that we should hold Petitioner to its alleged previous arguments in the companion district court lawsuit (Prelim. Resp. 2–26). We also discuss above Patent Owner's contentions regarding evidentiary weight to be given to Dr. Subramanian's Declaration (*id*. at 32–35). Patent Owner makes two additional arguments regarding obviousness of claim 1 over Dodd as

follows: (1) Dodd does not teach a copy of the clock signal going to the register circuit (*id*. at 35–37) and (2) Dodd does not teach a plurality of copies of the command and address signals (*id*. at 37–39).

Regarding the first of these, i.e., that Dodd does not teach a copy of the clock signal going to the register circuit (*id*. at 35–37), Patent Owner acknowledges that Dodd teaches Dodd's output clock 20 is provided to data buffers 123 and 124 (*id*. at 37). Patent Owner, however, contends that "this purported register circuit is the portion of the block 122 which holds the command and address data" and "we do not see any indication that the purported copy of the clock" is sent to "the other portion of block 122." *Id*. at 36–37.

Contrary to Patent Owner's contention (id.), Petitioner points to Dodd's teaching of a buffering structure, as discussed above. *See, e.g.*, Pet. 25 (citing *e.g.*, Ex. 1003, 2:40–45)). Consistent with Petitioner's contentions and Patent Owner's acknowledgement, Dodd teaches receiving copies of the clock signal by data buffers 123 and 124, within the buffering structure, e.g., buffer 120. *See, e.g.*, Ex. 1003, 5:57–6:11, Figs. 1, 3, 5. Second, consistent with Petitioner's contentions (*see, e.g.*, Pet. 26), Dodd teaches that clock circuit 300 is embedded within ADDR/CMD buffer 122, which temporarily stores address and command signals and also is within the buffering structure. Ex. 1003, 5:57–6:11, Figs. 1, 5.

Furthermore, we are not persuaded by Patent Owner's implicit contention that the recitation of "arrange[d] in a memory module in a common chip packing" in claim 1 requires that the register circuit

and clock signal regeneration circuit be within the same portion of a particular buffer. Prelim. Resp. 35–37. To the contrary, based on the current record at this juncture, the teachings of Dodd appear similar to at least one embodiment of a common chip packing described in the '150 Patent Specification (Ex. 1001, Fig. 2).

Regarding the second of Patent Owner's contentions, i.e., that Dodd does not teach a plurality of copies of the command and address signals (Prelim. Resp. 37–39), Patent Owner's contentions are based on a small portion of Dodd's teachings identified and explained in the Petition (Pet. 22–31), which are taken out of context. More specifically, Patent Owner bases its contentions on an alleged insufficiency of "two thick lines" in Figure 1 of Dodd. Prelim. Resp. 37–39. Petitioner, however, more broadly points to Dodd's teachings relating to buffer structures. *See, e.g.*, Pet. 28–31 (citing *e.g.*, Ex. 1003, 2:39–3:12, 3:51–4:18, 5:60–65, Figs. 1, 3, 5; Ex. 1011 ¶¶ 47–52). Consistent with Petitioner's contentions, Dodd teaches transmitting signals such as data, status information, address information and command information to the memory chips. Ex. 1003, 2:36–41, 2:54–63, 5:63–66. Dodd also teaches that the buffered structure allows for "bolder scaling" and that connection lines "represented as a single line" instead "may in fact be a plurality of lines." *Id*. at 2:48–56.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claim 1 to be unpatentable in

view of Dodd.

4. Discussion of Claims 2, 5, 6, and 8–10

Each of claims 2, 5, 6, and 8–10 depends directly from independent claim 1. We have reviewed Petitioner's showing (Pet. 32–39) with respect to dependent claims 2, 5, 6, and 8–10 and the teachings of Dodd.

Patent Owner contends that Dodd does not teach that the clock and register circuits are "integrated on a common chip," as recited in claim 5 or that the common chip packaging is "arranged essentially at a central position" on the memory module, as recited in claim 6. Prelim. Resp. 39–47. Patent Owner also disputes Petitioner's contentions regarding dependent claim 10. *Id*. at 48–50.

Regarding claim 5, Patent Owner's contentions are premised on whether the asserted art contains precisely the same words as the further recitation of claim 5. More specifically, Patent Owner asserts that the word "embedded" is too imprecise to teach "integrated on a common chip," based on various dictionary definitions of "embedded" and "encapsulate," some of which pertain to computer software. Prelim. Resp. 39 (citing Ex. 2005; Ex. 2006; Ex. 2007; Ex. 2008; Ex. 2009). Contrary to Patent Owner's assertion, Dodd pertains to buffering for memory devices, such as DRAM devices. Ex. 1003, 1:8–15. In this context, Dodd teaches "[w]ithin the ADDR/CMD buffer 122, there is embedded therein a clock circuit 300 and a clock driver 310." Id. at 6:1–3; *see also id*. at 3:64–65 ("Embedded in the ADDR/CMD buffer 122 is an embedded clock circuit 300."). Furthermore, dictionary definitions proffered

by Patent Owner that pertain to electronics are consistent with Petitioner's contentions, e.g., "to include within a larger entity" (Ex. 2005, 3). We disagree with Patent Owner's contention that we cannot consider teachings relied upon by Petitioner that do not include the exact term "integrated." Petitioner contends that claim 5 is obvious (Pet. 4), which involves a determination of whether the claimed invention would have been obvious to a person of ordinary skill in the art based on the *Graham* factors, not an *ipsissima verba* test.

Regarding claim 6, Patent Owner contends that we should not rely on Dr. Subramanian's testimony regarding figures of Dodd for the further recitation that the common chip packaging is "arranged essentially at a central position" on the memory module, as recited in claim 6 because the figures do not show a physical arrangement and the corresponding text of Dodd does not describe the placement using the exact words "central position." Prelim. Resp. 42–45. Based on the record before us, we are not persuaded that Dodd's figures cannot be considered at all with respect to a physical arrangement. Instead, we note that at least Figure 5 of Dodd specifically shows the buffering structure on memory module 150. Ex. 1003, Fig. 5. Furthermore, for the reasons discussed above with respect to claim 5, we are persuaded by Dodd's teachings, including pictorial representations of circuits, regardless of whether the exact term "central" is used.

Regarding claim 10 and the further recitation "wherein the memory module comprises an RDIMM module," Patent Owner, more specifically, contends that Dodd "disparages the use of RDIMMs." Prelim.

Resp. 48. Based on the record before us at this juncture, we find that Dodd's description of "[p]rior art designs" (Ex. 1003, 1:64–2:5) does not criticize, discredit, or otherwise discourage the use of its reliability improvements in connection with a RDIMM module. *See DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) ("A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not 'criticize, discredit, or otherwise discourage' investigation into the invention claimed.") (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)). Dodd teaches that its solution of reducing costs by embedding a clock signal (Ex. 1003, 6:63–67) may be used in "memory devices 130–145, such as DRAM devices" (*id*. at 2:47–48). Dodd further teaches that "many modifications may be made" and the embodiments are intended to be "illustrative and not restrictive" (*id*. at 7:3–15).

5. Discussion of claims 3 and 11

We next turn to dependent claims 3 and 11, each of which depends directly from independent claim 1. Petitioner asserts that the combination of Dodd and Keith teaches all elements of claims 3 and 11 and provides a rationale for combining the teachings of Dodd and Keeth. Pet. 39–41.

For instance, Petitioner contends that differential signaling was well-known and points to Keeth's teachings of memory devices using differential signaling for clock signals in DDR DRAM devices. Pet. 39 (citing Ex. 1016, 1:25–44; Ex. 1011 ¶¶ 65–67). Relying on the testimony of Dr.

Subramanian, Petitioner also asserts that one of ordinary skill would have used differential signaling with Dodd's clock signals and used a DDR DRAM device with the Dodd's reliability technique to improve performance and speed. *Id*. at 40–41 (citing Ex. 1016, 1:25–44; Ex. 1011 ¶¶ 65–67).

At this juncture of the proceeding, Petitioner has accounted sufficiently for the limitations of claims 3 and 11. Additionally, Petitioner has articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have modified Dodd's system so as to apply Keeth's teachings of DDR DRAM devices and using differential signaling for clock signals. Patent Owner does not argue for the separate patentability of claims 3 and 11 with respect to this challenge. Prelim. Resp. 35–50.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claims 3 and 11 to be unpatentable in view of Dodd and Keeth.

6. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–3, 5, 6, and 8–11 are unpatentable as obvious over Dodd alone or in combination with other art.

F. Obviousness over Lee alone or with Keeth

Petitioner contends claims 1, 2, 5, 6, and 8–10 are unpatentable under 35 U.S.C. § 103(a) as obvious over Lee. Pet. 41–52. Petitioner also

contends that claims 3 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Lee and Keeth. Pet. 52–54.

1. Overview of Lee

Lee is directed to a method for transmitting a command signal and an address signal, which includes buffering and then transmitting in response to a clock signal and a select signal. Ex. 1007, Abstract. Figure 4 is reproduced below.

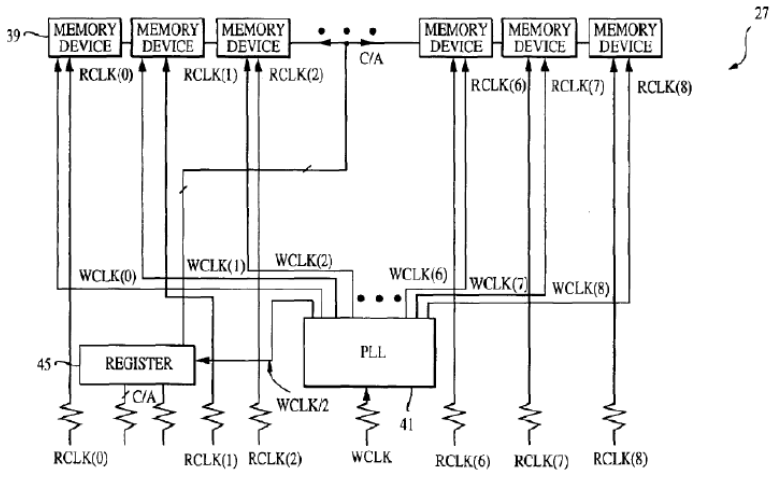

FIG. 4

Figure 4 illustrates Memory Subsystem 27

As shown in Figure 4 above, memory subsystem 27 includes write clock (WCLK) regeneration circuit 41, which is a phase lock loop (PLL) and provides WCLK (0) to WCLK (8) signals to each of individual DRAM memory devices 39. *Id.* at 7:26–30. Memory subsystem 27 also includes register 45, which receives a WCLK/2 signal from WCLK regeneration circuit 41 and command and address data (C/A). *Id.*

at 7:34–40.

2. Discussion of Claim 1

We begin our analysis with independent claim 1. Claim 1 is directed to a memory module comprising memory chips and bus lines. Ex. 1001, 7:1–7. Petitioner points to teachings relating to memory module 27. Pet. 41–48 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 69–71). Consistent with Petitioner's contentions (*id.*), Lee teaches that memory module 27 comprises memory chips 39 and bus lines (Ex. 1008, Figs. 1, 3, 4). Also consistent with Petitioner's teachings, in Lee's memory system 9 buses send signals, e.g., command and address signals to a plurality of memory modules 27 (*id.* at 4:1–14), each of which may be implemented as a DIMM (*id.* at 6:6–21, 7:26–27).

Claim 1 also recites a clock signal regeneration circuit configured to generate copies with the same frequency as the incoming clock signal and supply the copies to the memory chips. Ex. 1001, 7:8–13. Petitioner points to Lee's teachings relating to PLL 41 of memory module 27. Pet. 43 (citing Ex. 1008, 6:51–55; Fig. 4; Ex. 1011 ¶¶ 72–73). Consistent with Petitioner's contentions (*id.*), Lee teaches "[p]referably the clock regeneration circuit is formed as a zero delay phase lock loop (PLL) or low skew data buffer" (Ex. 1008, 6:51–55), which "receives the WCLK signal" and "provides a plurality of regenerated WCLK signals to the respective memory devices e.g., DRAMS 39, provided within memory subsystem 27" (*id.* at 6:47–50). Lee further "illustrates the WCLK regeneration circuit 41 as a (PLL) phase lock loop," which "provides the

respective WCLK signals WCLK(0) . . . WCLK(8) to each of the individual DRAM memory devices 39." *Id.* at 7:26–34.

Claim 1 additionally recites a register circuit arranged on the memory module in a common chip packing with the clock regeneration circuit and configured to receive copies of the clock signal from the clock regeneration circuit. Ex. 1001, 7:14–18. Petitioner points to Lee's teachings relating to module 27, comprising register 45 and PLL 41. Pet. 44–45 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 74–76). Relying on the testimony of Dr. Subramanian, Petitioner also contends that an ordinarily skilled artisan would have recognized that register 45 and PLL 41 would have been included in a single chip packing. *Id.* Consistent with Petitioner's contentions (id.), Lee teaches that memory module 27 may be implemented as a DIMM (Ex. 1008, 6:6–21, 7:26–27) and that memory module 27 includes register 45 and PLL 41 (*id.* at Fig. 4).

Claim 1 further recites that the register circuit is configured to temporarily store and then supply to the memory chips copies of command and address signals having the same frequency as the incoming command and address signals. Ex. 1001, 7:18–25. Petitioner points to Lee's teachings relating to register 45 temporarily storing command and address signals and then supplying copies of these signals to chips 39 under control of the WCLK signal. Pet. 46–48 (citing Ex. 1008, 7:35–41, 11:29–37, Fig. 4; Ex. 1003, Fig. 1; Ex. 1011 ¶¶ 78–80). Petitioner's contentions will be discussed further below with respect to Patent Owner's contentions.

We turn now to Patent Owner's contentions. Our claim construction discussion above addresses Patent Owner's contentions that we should hold Petitioner to its alleged previous arguments in the companion district court lawsuit (Prelim. Resp. 2–26). We also discuss above Patent Owner's contentions regarding evidentiary weight to be given to Dr. Subramanian's Declaration (*id*. at 32–35). Patent Owner makes three additional arguments regarding obviousness of claim 1 over Lee as follows: (1) Lee does not teach a copy of the clock signal having a same frequency going to the register circuit (*id*. at 50–52); (2) Lee does not teach a register circuit and clock circuit in a common chip packing (*id*. at 52–54); and (3) Lee does not teach a plurality of copies of the command and address signals (*id*. at 54–55).

We turn to the first of these, i.e., that Lee does not teach a copy of the clock signal having a same frequency going to the register circuit (Prelim. Resp. 50–52). Petitioner points to Lee's teaching of providing copies of signals to three exemplary memory devices on the left and three exemplary memory devices on the right (Pet. 46–48 (citing Ex. 1008, 7:35–42, 11:29–37, Fig. 4; Ex. 1003, Fig. 1; Ex. 1011 ¶¶ 79–80). Patent Owner contends that because Figure 4 of Lee shows a "WCLK/2" input to register 45, Lee fails to teach that the copies of the command and address signals have the same frequency as the incoming command and address signals. Prelim. Resp. 51.

As discussed above with respect to claim construction, "same frequency" is within a larger

phrase[7] and based on the record before us at this juncture, we decline to construe the full phrase such that both the generated copies and the copies that are supplied are required to be at the same frequency as the incoming signals. Consistent with Petitioner's contentions (Pet. 46–48), Lee teaches that the supply of command and address signals to memory devices 39 is at the same frequency as the incoming signals (Ex. 1004, Fig. 4).

Additionally, as discussed above with respect to claim construction, in the Summary of the Invention, the '150 Patent describes that "CA signals are multiplied by a factor of 1:X" so that "several CA copies can be provided to several branches." Ex. 1001, 2:57–59; *see also id.* at 3:61–64 ("The register and clock signal regeneration circuits are, *preferably*, designed such that they each multiply the clock signal and the command and address signal by a factor of 1:2" (emphasis added)). Lee's teaching is similar to this description in the '150 Patent Specification as in both cases the frequency is adjusted by a factor of 1:2 due to a branch in the circuit. *Compare* Ex. 1001, 2:57–59, 3:61–64 *with* Ex. 1008, Fig. 4.

Lee includes further teachings consistent with Petitioner's contention. For instance, Lee teaches that "PLL 41" is "used to *regenerate*" the local clock

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[7] Claim 1 recites that the register circuit is configured "to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having *a same frequency* as the incoming command and address signals." Ex. 1001, 7:18–25.

signal (*id*. at 7:34–41 (emphasis added)); that command and address data are provided by "*regenerating* an additional data write clock signal" (*id*. at 11:32–35 (emphasis added)); and that the frequency of the additional data write clock signal may be at a frequency of "X/N where X is the frequency of said received data write clock signal and N is an integer" (*id*. at 11:38–41). We further note with respect to the last of these that because "1" is an integer, when "N" is "1" the same frequency is used.

Regarding the second of Patent Owner's contentions, i.e., that Lee does not teach a register circuit and clock circuit in a common chip packing (Prelim. Resp. 52–54), Patent Owner contends that "Petitioner appears to admit that Lee does not show the register circuit and clock circuit in a common chip packaging" (*id*. at 52). Based on the record before us at this juncture, we do not agree with Patent Owner's characterization of Petitioner's contentions.

However, even if we agreed with Patent Owner's characterization, we are persuaded by Petitioner's contentions (Pet. 44–45 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 74–76)) that it would have been obvious in view of Lee's teachings, including Figure 4, to place register 45 and PLL 41 in a common chip packing. Patent Owner contends that Petitioner asserts "a 'design choice' theory against limitations that are touted as significant aspects of the invention" and that "the Board cannot find that a patent is *per se* obvious merely because there is a rearrangement of parts found in the prior art." Prelim. Resp. 53 (citing *Cutsforth, Inc. v. Motivepower, Inc*., 636 Fed. App'x

575, 578 (Fed. Cir. 2016) (nonprecedential)).

In the instant proceeding, contrary to Patent Owner's contention, Petitioner's obviousness contention (Pet. 41–45) does not involve a rearrangement of parts. Consistent with Petitioner's contention, Lee teaches that "FIG. 4 illustrates in greater detail a memory subsystem 27, which as noted, may be a DIMM memory device." Ex. 1007, 7:26–27. Figure 4 shows that memory module 27 has "REGISTER" 45 and "PLL" 41. *Id*. at Fig. 4. Additionally, Dr. Subramanian points to Lee's teachings regarding "one-chip memory" or "a chip set" as evidence supporting his testimony that these two design choices (i.e., packaged either together or separately) would have been known to a person of ordinary skill in the art. *Id*. at 8:26–27 (cited in Ex. 1011 ¶ 75).

Regarding the third of Patent Owner's contentions, i.e., that Lee does not teach a plurality of copies of the command and address signals (Prelim. Resp. 54–55), Patent Owner's contention, more specifically, is based on "one line labeled C/A coming out of" register 45 (*id*. at 55). Consistent with Petitioner's contentions (Pet. 46–48), Lee teaches regenerating the WCLK signal "to control capture of the command and address signals" received by "register 45 which clocks in the command and address data" (Ex. 1008, 7:34–40). Figure 4 of Lee also includes a "C/A" label at the top of Figure 4 illustrating providing command and address signals to three memory devices on the left-hand side and three memory devices on the right-hand side. *Id*. at Fig. 4. Additionally, Lee teaches generating and supplying a plurality of copies of the write clock

signal (*see, e.g., id.* at 7:26–34), which control data read and write operations (*id.* at 4:42–44). Furthermore, Lee is directed to "a clocking system and method for effecting high speed data transfers" (*id.* at 1:10–12) and specifically teaches providing command and address (C/A) signals to a plurality of memory storage devices via a register (*id.* at 4:1–14, 7:34–41, 11:4–41, Fig. 4).

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claim 1 to be unpatentable in view of Lee.

3. Discussion of Claims 2, 5, 6, and 8–10

Each of claims 2, 5, 6, and 8–10 depends directly from independent claim 1. We have reviewed Petitioner's showing (Pet. 48–52) with respect to dependent claims 2, 5, 6, and 8–10 and the teachings of Lee.

Patent Owner contends that Lee does not teach that the clock and register circuits are "integrated on a common chip," as recited in claim 5 or that the common chip packaging is "arranged essentially at a central position" on the memory module, as recited in claim 6. Prelim. Resp. 56–57. Regarding claim 5, consistent with Petitioner's contentions (Pet. 32–33), Lee, for example, teaches that memory module 27 includes register 45 and PLL 41 (Ex. 1008, Fig. 4). Additionally, Dr. Subramanian testifies that a person of ordinary skill in the art would have understood from Figure 4 of Lee that register 45 and PLL 41would be included in a single chip pack. Ex.

1011 ¶¶ 74–76. Regarding claims 5 and 6, Dr. Subramanian also testifies that integrating the clock signal regeneration circuit and register circuit on a common chip and placing the common chip packaging in a central location would have been obvious to a person of ordinary skill in the art. *Id.* ¶¶ 74–76, 83–84.

For claim 5, Patent Owner refers back to its contentions for claim 1 and asserts that because Lee does not teach common chip packaging, Lee also does not teach integrating the register circuit and clock regeneration circuit on a common chip. Prelim. Resp. 56. For claim 6, Patent Owner references back to its contentions for Dodd and again asserts that Lee does not show a physical arrangement. *Id.* For the same reasons given above, we are persuaded by Petitioner's contentions even after full consideration of Patent Owner's assertions.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claims 2, 5, 6, and 8–10 to be unpatentable in view of Lee.

4. Discussion of claims 3 and 11

We next turn to dependent claims 3 and 11, each of which depends directly from independent claim 1. Petitioner asserts that the combination of Lee and Keith teaches all elements of claims 3 and 11 and provides a rationale for combining the teachings of Lee and Keeth. Pet. 52–54. Petitioner points to the same portions of Keeth discussed above with respect to the first set of challenges (based on Dodd and

Keeth). Again, relying on the testimony of Dr. Subramanian, Petitioner also asserts that one of ordinary skill would have used differential signaling with Lee's clock signals and used a DDR DRAM device with the Lee's technique to improve performance and speed. *Id*. (citing Ex. 1016, 1:25–44; Ex. 1011 ¶¶ 89–91).

At this juncture of the proceeding, Petitioner has accounted sufficiently for the limitations of claims 3 and 11. Additionally, Petitioner has articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have modified Lee's system so as to apply Keeth's teachings of DDR DRAM devices and using differential signaling for clock signals. Patent Owner does not argue for the separate patentability of claims 3 and 11 with respect to this challenge. Prelim. Resp. 50–58.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claims 3 and 11 to be unpatentable in view of Lee and Keeth.

5. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–3, 5, 6, and 8–11 are unpatentable as obvious over Lee alone or in combination with other art.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable

likelihood that Petitioner would prevail in showing that claims 1–3, 5, 6, and 8–11 of the '150 Patent are unpatentable. At this preliminary stage, we have not made a final determination with respect to the patentability of the challenged claims or any underlying factual and legal issues.

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–3, 5, 6, and 8–11 of the '150 Patent on the following grounds of unpatentability:

Reference(s)	**Basis**	**Challenged Claim(s)**
Dodd	§ 103(a)	1, 2, 5, 6, and 8–10
Dodd and Keeth	§ 103(a)	3 and 11
Lee	§ 103(a)	1, 2, 5, 6, and 8–10
Lee and Keeth	§ 103(a)	3 and 11

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision; and

FURTHER ORDERED that the trial is limited to the grounds identified immediately above, and no other ground is authorized.

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APPENDIX G

Trials@uspto.gov Paper 31
571-272-7822 Entered: February 13, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE
PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,
v.
POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2017-00116
Patent 7,334,150 B2

Before SALLY C. MEDLEY, BARBARA A. PARVIS, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–3, 5, 6, and 8–11 ("challenged patents") of U.S. Patent No. 7,334,150 B2 (Ex. 1001, "the '150 Patent"). Paper 2 ("Pet."). In support of its Petition, Petitioner proffers a Declaration of Dr. Vivek Subramanian. Ex. 1011. Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). Upon consideration of the parties' contentions and supporting evidence, we instituted an *inter partes* review pursuant to 35 U.S.C. § 314, as to claims 1–3, 5, 6, and 8–11 of the '150 Patent. Paper 9 ("Dec.").

Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 17, "PO Resp."). In support of its Patent Owner Response, Patent Owner proffers the Declaration of Dr. Joseph Bernstein. Ex. 2019. Petitioner filed a Reply to Patent Owner's Response (Paper 20, "Pet. Reply"). On December 6, 2017, we held an oral hearing. Paper 30 ("Tr.").

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3, 5, 6, and 8–11 of the '150 Patent are unpatentable.

A. Related Matters

The parties state that the '150 Patent is the subject of a pending lawsuit in the Central District of California, i.e., *Polaris Innovations Ltd. v. Kingston Tech. Co.*, Case No. 8:16–cv-300 (C.D.

Cal.),[1] and the lawsuit includes assertions against Petitioner. Pet. 2; Paper 3 (Patent Owner's Mandatory Notices), 1; Paper 16 (Patent Owner's Supplemental Mandatory Notices).

B. The '150 Patent

The '150 Patent is directed to a semiconductor memory module that includes a register circuit and a clock signal regeneration circuit. Ex. 1001, 1:9–16. Figure 2 is reproduced below.

[1] This lawsuit is referred to herein as the "companion district court lawsuit."

142a

FIG 2

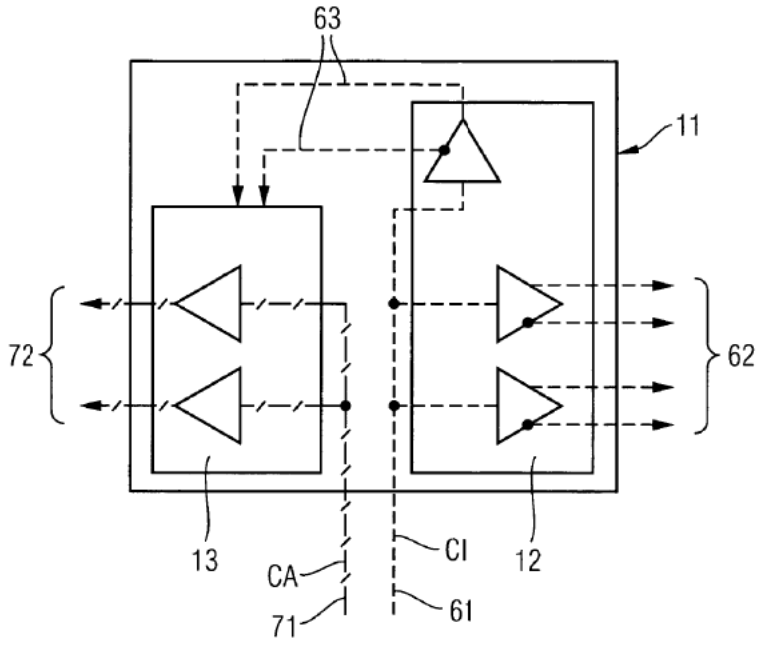

Figure 2 shows a top view of a clock signal regeneration circuit and register circuit in a common chip packing.

As shown in Figure 2 above, chip packing 11 contains clock signal regeneration circuit 12 and register circuit 13. Ex. 1001, 4:30–33. Differential clock signal input line 61 supplies clock signal Cl to common chip packing 11. *Id*. at 4:41–43. Line section 71 supplies command and address input signals "CA." *Id*. at 4:43–45. Differential clock signal lines 62 from clock signal regeneration circuit 12 supply the

conditioned clock signal to memory chips 4 and 4a. *Id*. at 4:49–53. Differential clock signal lines 63 supply the conditioned clock signal to register circuit 13. *Id*. at 4:54–56. From register circuit 13, temporarily stored command and address signals are supplied by differential command and address signal lines 72 to memory chips 4 and 4a. *Id*. at 4:56–60.

C. Illustrative Claim

Petitioner challenges claims 1–3, 5, 6, and 8–11 of the '150 Patent. Claim 1 is an independent claim. Claims 2, 3, 5, 6, and 8–11 depend directly from claim 1. Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A memory module comprising:
>
> a plurality of memory chips arranged on the memory module;
>
> a plurality of bus signal lines operable to supply an incoming clock signal and incoming command and address signals to at least the memory chips;
>
> a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to supply the copies of the incoming clock signal to the memory chips, the copies of the incoming clock signal having a same frequency as the incoming clock signal; and
>
> a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and configured to receive one of the copies of the incoming clock signal from the clock regeneration

> circuit, the register circuit being further configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a same frequency as the incoming command and address signals.

Id. at 7:1–25.

D. Instituted Grounds of Unpatentability

Petitioner asserts that claims 1–3, 5, 6, and 8–11 are unpatentable based on the following grounds (Pet. 4):

Reference(s)	**Basis**	**Challenged Claim(s)**
Lee[2]	§ 103(a)	1, 2, 5, 6, and 8–10
Lee and Keeth	§ 103(a)	3 and 11
Dodd[3]	§ 103(a)	1, 2, 5, 6, and 8–10
Dodd and Keeth[4]	§ 103(a)	3 and 11

We instituted on all of the asserted grounds of unpatentability above. Dec. 33.

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[2] U.S. Patent No. 6,898,726 B1, issued May 24, 2005 (Ex. 1008) ("Lee").

[3] U.S. Patent No. 6,530,006 B1, issued Mar. 4, 2003 (Ex. 1003) ("Dodd").

[4] U.S. Patent No. 7,123,046 B2, issue Oct. 17, 2006 (Ex. 1016) ("Keeth").

II. DISCUSSION

A. Overview

A patent claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

B. Person of Ordinary Skill in the Art

Petitioner proposes that a person of ordinary skill in the art had a Master's degree in Electrical Engineering and at least 2 years' experience working in the field of semiconductor memory design. Pet. 7 (citing Ex. 1011 ¶¶ 17–19). Patent Owner counters that the person of ordinary skill in the art "would only have had a Bachelor's degree, or the equivalent, in the art of semiconductor memory module design." PO Resp. 4–5 (citing Ex. 2019 ¶¶ 24–30).

The dispute centers on Patent Owner's

contention that a person of ordinary skill would have lacked familiarity with components of memory modules and technical differences between RDIMMs and other memory modules, and further would have had ordinary creativity that "coexisted" with "his or her status" as a "junior member of the team." *Id*. Patent Owner's contention regarding the lack of familiarity of the skilled artisan with prior art teachings, e.g., technical differences between RDIMMs and other memory modules, is contrary to legal precedent that a person of ordinary skill in the art is presumed to be aware of all pertinent prior art. *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 454 (Fed. Cir. 1985).

Regarding the level of skill, we consider the level of skill implied by the disclosures of the prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of skill in the art). For the reasons given below, upon consideration of the Petition, the Patent Owner Response, the Petitioner's Reply, and the evidence cited therein, we adopt Petitioner's proposed level of skill as consistent with the evidence of record. We credit Dr. Subramanian's testimony regarding level of skill as consistent with the evidence of record, including the disclosures of the prior art references and the level of skill implied by these disclosures. We, however, note that based on the complete trial record, our findings and conclusion would be the same under either proposal.

C. Claim Construction

Petitioner provides proposed constructions for

certain terms. Pet. 12–17. In Patent Owner's Preliminary Response, Patent Owner countered and presented additional contentions regarding claim construction. *See, e.g.*, Prelim. Resp. 4–32. In our Institution Decision, we determined that neither "clock signal regeneration circuit" nor "a register . . . configured to . . . generate a plurality of copies of the incoming command and address signals" invokes § 112 ¶ 6.[5] Dec. 7–9. We further determined that no express interpretation was necessary of these phrases. *Id.* We also were not persuaded that Petitioner should be held to previous arguments in the companion district court lawsuit that claim 6 is indefinite. *Id.* at 9. The parties do not challenge the determinations in the Institution Decision. *See e.g.*, PO Resp 43–62; Pet. Reply 14–22. Based on the entire trial record before us, we see no need to change these determinations.

In our Institution Decision, we also made determinations regarding the terms "having a same frequency" and "RDIMM." *Id.* at 10–12. Patent Owner's disputes in its Patent Owner Response implicitly pertain to the construction of these terms, so we provide further analysis regarding construction of these terms below.

1. "having a same frequency"

In the Petition, Petitioner contends that "having

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[5] Section 4(c) of the Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA") re-designated 35 U.S.C. § 112 ¶ 6, as 35 U.S.C. § 112(f). Because the '150 Patent has a filing date before September 16, 2012, the effective date of § 4(c) of the AIA, we will refer to the pre-AIA version of 35 U.S.C. § 112.

a same frequency" means "with no intended modification from the frequency of the incoming signal." Pet. 13–16. In the Institution Decision, we considered Patent Owner's contention that "intended" interjects a vague term and should be removed from Petitioner's proposed construction. Dec. 10–12 (citing Prelim. Resp. 28–31).

At the institution stage, we did not adopt the proposal of either party. We noted that "same frequency" is within larger phrases recited in independent claim 1. Dec. 11–12. We declined to construe the phrase "having a same frequency" such that both the generated copies and the copies supplied are required to be at the same frequency as the incoming signals. We explained that our determination was based on embodiments set forth in the '150 Patent Specification. *Id*. (citing Ex. 1001, 2:57–59, 3:61–63). We further determined no other express construction of the term "same frequency" is needed to resolve a dispute between the parties.

In its Patent Owner Response, Patent Owner contends "Lee's WCLK/2 signal operates at a different frequency from WCLK, so it cannot be a 'copy' of the WCLK having the same frequency as WCLK, as claimed." PO Resp. 45. Patent Owner's contentions in its Patent Owner Response pertain to only the "signal WCLK/2" that is supplied to register 45. *Id*. at 43–47. In particular, claim 1 recites "a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and *configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit*." Ex. 1001, 7:14–18 (emphases added). Patent Owner's contentions are premised on "one of *the*

copies of the incoming clock signal" having antecedent basis in "the copies of the incoming clock signal having a same frequency as the incoming clock signal." *Id.*

Petitioner contends that the "clock signal regeneration circuit" limitation requires only the copies supplied to the memory chips to "hav[e] a same frequency as the incoming clock signal," and that the omission of that language from the "register circuit" limitation indicates that the copy of the incoming clock signal that the register circuit is configured to receive need not have the same frequency as the incoming clock signal. Reply 15–16. According to Petitioner, "each and every one of the 'same frequency' copies that are generated by the clock signal regeneration circuit are supplied to the memory chips." Reply 15; Pet. 43–48. Petitioner further contends that "the register simply needs to be 'configured to,' i.e., able to receive a copy of the clock signal" and, "[a]s long as the register is so configured, the claim limitation is met regardless of whether the copy of incoming signal sent to the register has the same frequency or not." Reply 16–17.

Upon consideration, consistent with Petitioner's proposal, we are persuaded that the "the copies of the incoming clock signal" that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory chips" must have the same frequency as the incoming clock signal. We are not persuaded that the "one of the copies" that the register circuit is configured to receive must have the same frequency as the incoming clock signal as argued by the Patent Owner. Our determination is consistent with the express recitations in claim 1 and the intrinsic

evidence. For instance, the recitation of "having a same frequency" in claim 1 immediately follows the supply of signals to the memory chips.

> a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to *supply the copies* of the incoming clock signal *to the memory chips*, the copies of the incoming clock signal *having a same frequency* as the incoming clock signal; and
>
> a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit, the register circuit being further configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and *supply the copies* of the incoming command and address signals *to the memory chips*, the copies of the incoming command and address signals *having a same frequency* as incoming command and address signals.

Ex. 1001, 7:8–25 (emphases added).

Importantly, if we were to adopt Patent Owner's proposal, then the claim would require "one of the copies of the incoming clock signal from the clock regeneration circuit" received by the register circuit also be supplied to at least one of the memory chips. Upon consideration of the contentions of both parties, we are not persuaded that such an interpretation is

consistent with the express language of claim 1 or the intrinsic evidence, including the '150 Patent Specification.

Furthermore, based on the entire trial record, the intrinsic evidence, including the '150 Patent Specification, supports that the "one of the copies of the incoming clock signal from the clock regeneration circuit" need not have the same frequency as the incoming clock signal. Petitioner contends (Pet. 13–15) and Patent Owner does not dispute (Prelim. Resp. 28–31; PO Resp. 43–47) that the phrase "having the same frequency" did not appear in the Specification or claims as filed, but was added by amendment. Neither party points us to disclosure in the '150 Patent Specification requiring that "having the same frequency" pertains to "one of the copies of the incoming clock signal from the clock regeneration circuit."

Additionally, as we explained in the Institution Decision (Dec. 11–12), in embodiments set forth in the '150 Patent Specification, including a preferred embodiment, "[t]he register and clock signal regeneration circuits are, preferably, designed such that they each multiply the clock signal and the command and address signal by a factor of 1:2" (Ex. 1001, 3:61–63) such that "several" copies "can be provided to *several DRAM branches or channels*" (*id.* at 2:57–59 (emphasis added).) Additionally, the Detailed Description of the '150 Patent also describes multiplying these signals so as to supply chip-groups.

> [I]ncoming clock signal C1 is conditioned and the incoming command and address signals

> CA are temporarily stored in order to multiply these signals by a factor of 1:X and *to supply the conditioned clock signal C1 and the temporarily stored command and address signals CA to X semiconductor memory chip groups* that are arranged on the semiconductor memory module.

Ex. 1001, 5:67–6:6 (emphasis added).

Relying on the testimony of Dr. Bernstein and Dr. Subramanian, Patent Owner contends "when the '150 Patent states that signals are 'multiplied,' a POSITA would understand that to mean that copies of the signal are made." PO Resp. 15 n.3 (citing Ex. 2019 ¶ 65), 45 (citing Ex. 1011 ¶ 23; Ex. 2019 ¶ 66). More specifically, Dr. Bernstein testifies

> The '150 Patent makes numerous references to multiplying a signal by a factor of 1:X. *See id.* at 2:46, 2:47–51, 2:58, 6:19, 6:31. As one of ordinary skill in the art, I understand this terminology to mean that the signal is copied "X" number of times. This is clear given the overall focus of the '150 Patent on avoiding sending multiple copies of the CA signal. "Since the CA signals are multiplied by a factor of 1:X, several CA copies can be provided to several DRAM branches or channels." *Id.* at 2:57–59. The '150 Patent also uses this convention and fills in the "X" with the number "2" to describe an embodiment where two copies of signals are generated. *See id.* at 5:28–38 (describing Figure 3 illustrating two copies of by the CA line and the CL line). The fact that this

> terminology is referring to copying the incoming signal is made most evident by the statement that the register stores the CA signals "in order to multiply these signals by a factor of 1:X and to supply the conditioned clock signal Cl and the temporarily stored command and address signals CA to X semiconductor memory chip groups arranged on the semiconductor memory module." *Id.* at 6:2–6. This confirms that "X" in this notation means the number of copies that need to be made in order to send the signal to "X" groups of semiconductor chips. To be clear I find no suggestion that 1:X refers to multiplying the frequency of the signal X.

Ex. 2019 ¶ 66.[6]

As set forth above, Dr. Bernstein testifies that the '150 Patent Specification describes multiplying signals, which means that the signals are copied, so as to supply signals to "several DRAM branches or channels" or "to supply the conditioned clock signal Cl and the temporarily stored command and address signals CA to X semiconductor memory chip groups arranged on the semiconductor memory module." *Id.* (citing Ex. 1001, 2:57–59, 6:2–6). These embodiments

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[6] Patent Owner includes only cursory statements and a citation to this testimony by Dr. Bernstein. *See* PO Resp. 15 n.3 (citing Ex. 2019 ¶ 65), 45 (citing Ex. 1011 ¶ 23; Ex. 2019 ¶ 66 ("Dr. Subramanian and Dr. Bernstein agree that when the '150 Patent states that signals are "multiplied," a POSITA would understand that to mean that copies of the signals are made.") The Patent Owner Response must include "a detailed explanation of the significance of the evidence." *See* 37 C.F.R. §§ 42.22, 42.23, 42.120. Such detailed explanation is not provided.

(*id.*), however, are consistent with Petitioner's contentions regarding the scope of claim 1 (Reply 15; Pet. 43–48). Patent Owner does not point us to testimony of Dr. Bernstein indicating that claim 1 does not encompass these embodiments. Dr. Bernstein's testimony regarding finding "no suggestion that 1:X refers to multiplying the frequency of the signal" immediately follows and pertains to his testimony regarding sending or supplying signals "to 'X' groups of semiconductor chips." Ex. 2019 ¶ 66. We find Dr. Bernstein's testimony consistent with our determination in the Institution Decision that only "the copies of the incoming clock signal" that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory chips" must have the same frequency as the incoming clock signal.

Patent Owner also relies on the declaration testimony and deposition testimony of Dr. Subramanian. PO Resp. 43–45 (citing Ex. 1011 ¶ 23; Ex. 2018, 126:1–23). We do not find either supports Patent Owner's position. Dr. Subramanian's deposition testimony in this regard refers to "the limitation above" and does not include further explanation. Ex. 2018, 126:1–23. The limitation above recites the "clock signal regeneration circuit configured to . . . supply the copies of the incoming clock signal to the memory chips." Ex. 1001, 7:8–18. Additionally, Dr. Subramanian's declaration testimony is based on his analysis of the intrinsic evidence, including the '150 Patent Specification. *See, e.g.*, Ex. 1011 ¶¶ 23, 29, 30, 72–80. As discussed further below, Dr. Subramanian discusses the intrinsic evidence and claim construction and

concludes that Lee discloses the register circuit "configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit." Ex. 2018, 126:1–23.

For this Decision, we discern no reason to modify our analysis or our claim construction determination set forth in the Institution Decision regarding "having a same frequency." Based on the entire trial record, we determine that only "the copies of the incoming clock signal" that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory chips" must have the same frequency as the incoming clock signal. We, however, determine that the broadest reasonable interpretation of the "register circuit" limitation does not require that the "one of the copies of the incoming clock signal from the clock regeneration circuit" received by the register circuit has the same frequency as the incoming clock signal.

2. "RDIMM"

Petitioner contends that "RDIMM" stands for registered dual in line memory module. Pet. 17. Dr. Subramanian testifies that although "[t]he term 'RDIMM' appears twice" in the '150 Patent Specification, neither of these uses "defines or limits the meaning of the term 'RDIMM.'" Ex. 1011 ¶ 31. Dr. Subramanian also testifies that a RDIMM "is 'a Dual In-Line Memory Module that has register circuitry to buffer control signals.'" *Id*. ¶ 32.

Patent Owner agrees that "RDIMM" stands for registered dual in line memory module and, further, agrees that RDIMM's were known prior art devices. Prelim. Resp. 48; PO Resp. 10–14, 61. Patent Owner,

however, contends "RDIMMs are a well-known commercial DIMM type, which, among other things, buffers its C/A [command and address] signals, but not its data signals." PO Resp. 61 (citing a printout of a Dell Support webpage titled "PowerEdge: What are the different types of memory DIMMS for servers?" (Ex. 2034) ("**Registered DIMM**: RDIMM, buffers add, control, clock lines but does not buffer data I/O lines")). Dr. Bernstein testifies "RDIMMs feature a design that addresses performance issues . . . by putting a register between the memory controller and the memory devices on *only the command/address line*." Ex. 2019 ¶ 55 (emphasis added). Additionally, Patent Owner points to Dr. Subramanian's testimony that traditionally a fully buffered DIMM provides buffering for control signals and data signals. PO Resp. 12 (citing Ex. 2018, 19:7–11).

As an initial matter, a Web Page from Dell's Web Site with a print date of July 10, 2017, and a last modified date of May 31, 2017, is less probative than a definition or usage contemporaneous with the filing date of December 3, 2004 of the '150 Patent. Ex. 2034. Regarding the declaration and deposition testimony identified by the parties (Ex. 1011 ¶¶ 31–32; Ex. 2019 ¶ 55; Ex. 2018, 19:7–11), we need not make a determination regarding the broadest reasonable interpretation of RDIMM because based on the entire trial record, for the reasons set forth *infra* in Section II.D.3, we are persuaded that Petitioner shows sufficiently that Lee teaches an "RDIMM" even if we were to adopt Patent Owner's proposal that RDIMM stands for registered dual in line memory module, which buffers control signals,

but not data signals. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("[C]laim terms need only be construed 'to the extent necessary to resolve the controversy'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Obviousness over Lee alone or with Keeth

Petitioner contends claims 1, 2, 5, 6, and 8–10 are unpatentable under 35 U.S.C. § 103(a) as obvious over Lee. Pet. 41–52. Petitioner also contends that claims 3 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Lee and Keeth. Pet. 52–54.

1. Overview of Lee

Lee is directed to a method for transmitting a command signal and an address signal, which includes buffering and then transmitting in response to a clock signal and a select signal. Ex. 1007, Abstract. Figure 4 is reproduced below.

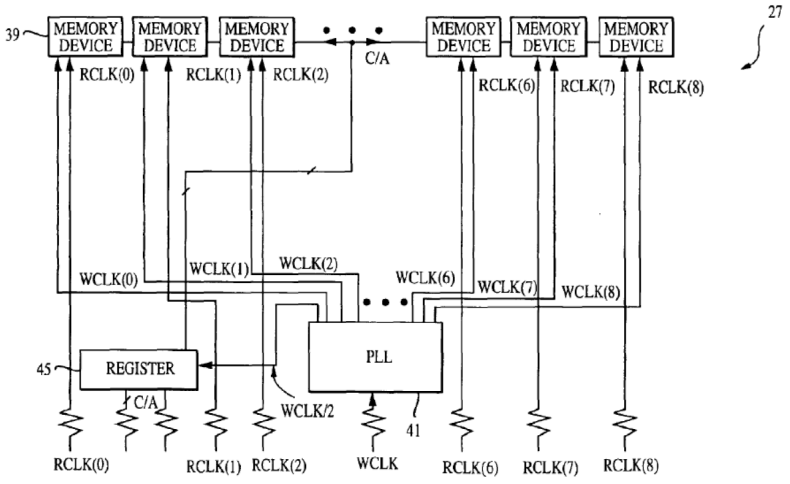

FIG. 4
Figure 4 illustrates Memory Subsystem 27

As shown in Figure 4 above, memory subsystem 27 includes write clock (WCLK) regeneration circuit 41, which is a phase lock loop (PLL) and provides WCLK (0) to WCLK (8) signals to each of individual DRAM memory devices 39. *Id*. at 7:26–30. Memory subsystem 27 also includes register 45, which receives a WCLK/2 signal from WCLK regeneration circuit 41 and command and address data (C/A). *Id*. at 7:34–41.

2. Overview of Keeth

Keeth is directed to adaptively adjusting a transition threshold of a data receiver using differential clock signals and a reference voltage. Ex. 1016, Abstract. According to Keeth, Double Data Rate Dynamic Random Access Memory (DDR DRAM) devices use differential signaling for clock signals at clock pins of a device package. *Id*. at 1:22–30. DDR DRAM devices use non-differential signaling for data

signals input on the device data pins. Id. at 1:35–37.

3. Discussion of Claim 1

a. The Petition—Claim 1

We begin our analysis with independent claim 1. Claim 1 is directed to a memory module comprising memory chips and bus lines operable to supply incoming clock and command and address signals to the memory chips. Ex. 1001, 7:1–7. Petitioner points to teachings relating to memory module 27. Pet. 41–48 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 69–71). Consistent with Petitioner's contentions (*id.*), Lee teaches that memory module 27 comprises memory chips 39 and bus lines (Ex. 1008, Figs. 1, 3, 4). Dr. Subramanian testifies that Lee's memory module 27 has a plurality of bus signal lines to supply incoming clock signal (WCLK) and incoming command and address signals (C/A) to memory chips 39. Ex. 1011 ¶ 71. We are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony (Pet. 41–48; Ex. 1011 ¶¶ 69–71), for example, because in Lee's memory system, 9 buses send signals, e.g., command and address signals and clock signals, to a plurality of memory modules 27 (Ex. 1008, 4:1–14, Figs. 1, 4). Each memory module 27 may be implemented as a DIMM. *Id*. at 6:6–21, 7:26–27. These contentions are not contested by Patent Owner. PO Resp. 43–56.

Claim 1 also recites "a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to supply the copies of the incoming clock signal to the memory chips, the copies of the incoming clock signal having the same frequency as the incoming clock signal." Ex. 1001, 7:8–13. Relying on the testimony of Dr.

Subramanian, Petitioner contends that Lee's PLL 41 of memory module 27 generates a plurality of copies of incoming clock signal CLK, i.e., WCLK (1–8), and supplies the copies to memory chips 39. Pet. 43 (citing Ex. 1008, 6:51–55; Fig. 4; Ex. 1011 ¶¶ 72–73). We are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony (*id*.) that Lee's clock signal regeneration circuit (PLL 41) generates a plurality of copies of the incoming clock signal and supplies the copies of the incoming clock signal to the memory chips because Petitioner's showing and Dr. Subramanian's testimony are consistent with Lee's teachings (see, e.g., Ex. 1008, Fig. 4). Patent Owner does not dispute Petitioner's contentions that Lee's clock signal regeneration circuit (PLL 41) generates a plurality of copies of the incoming clock signal and supplies the copies of the incoming clock signal to the memory chips. PO Resp. 43–56.

Regarding the remainder of the recitation, i.e., "the copies of the incoming clock signal having a same frequency as the incoming clock signal" (Ex. 1001, 7:11–12), we discuss this recitation in connection with the next recitation of "a register circuit" that is

> configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a same frequency as the incoming command and address signals.

Id. at 7:18–25.

As discussed *supra* Section II.C.1 with respect to claim construction, in each of these phrases, we determine that the "copies of the incoming command and address signals" that the register circuit is "configured . . . to generate . . . and supply . . . to the memory chips" must have the same frequency as the incoming signal. We, however, are not persuaded that the "one of the copies of the incoming clock signal from the clock regeneration circuit" must have the same frequency as the incoming clock signal.

Notwithstanding Patent Owner's contentions regarding this limitation, discussed further below, we are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony that Lee teaches (1) the clock signal regeneration circuit supplying copies of the incoming clock signal having a same frequency as the incoming signals; and (2) the register circuit supplying copies of the command and address signal having the same frequency as the incoming command and address signals. Pet. 43, 46–48 (citing Ex. 1008, 6:51–55, 7:35–42, 11:29–37, Fig. 4; Ex. 1003, Fig. 1; Ex. 1011 ¶¶ 73, 79–80). We are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony (*id*.) because they are consistent with the evidence cited therein including, for example, Figure 4 of Lee reproduced below.

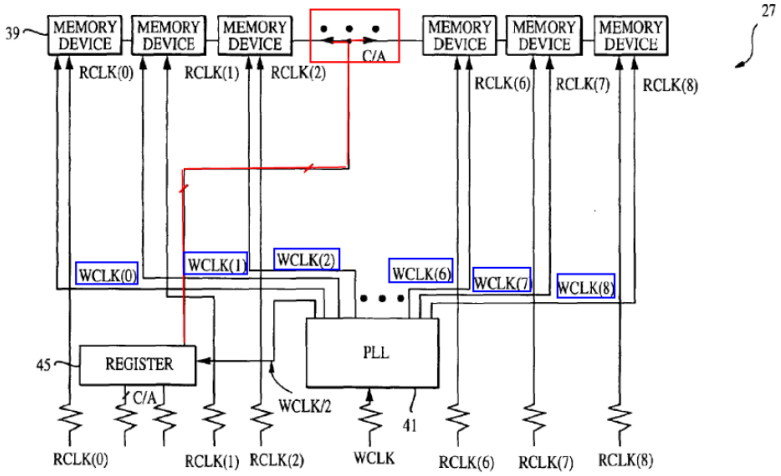

FIG. 4

Figure 4 illustrates Memory Subsystem 27 with Annotations by the Board

In the annotated version of Lee's Figure 4 reproduced above, we have added blue annotations showing copies of the incoming clock signal, i.e., WCLK(0) through WCLK (8) leaving PLL41 and red annotations showing copies of the command and address signal, i.e., C/A leaving register 45. Regarding the recitation in claim 1 of the "clock signal regeneration circuit" supplying "copies of the incoming clock signal" "having a same frequency" as the incoming signals (Ex. 1001, 7:8–12), Dr. Subramanian testifies that Lee teaches that PLL 41 generates copies of incoming clock signal, namely WCLK 1–8, and supplies those copies to memory chips 39 and that each of the copies have the same phase as input clock WCLK. Ex. 1011 ¶¶ 72, 73 (citing Ex. 1008, 6:51–55, Fig. 4). We credit Dr. Subramanian's testimony (id.) because it is

consistent with Lee's Figure 4 illustrating PLL 41 generating WCLK (0) through WCLK (8) (shown in blue annotations in Figure 4 above) and Lee's teaching that "[p]referably the clock regeneration circuit is formed as a zero delay phase lock loop (PLL)" so as to ensure "the regenerated WCLK signals having substantially the same phase as one another and as the phase of the WCLK signal on line 19." Ex. 1008, 6:51–55, Fig. 4. Additionally, Lee teaches "the clock regeneration circuit" "receives the WCLK signal" and "provides a plurality of regenerated WCLK signals to the respective memory devices e.g., DRAMS 39, provided within memory subsystem 27" (*id*. at 6:47–55). Lee further "illustrates the WCLK regeneration circuit 41 as a (PLL) phase lock loop," which "provides the respective WCLK signals WCLK(0) . . . WCLK(8) to each of the individual DRAM memory devices 39." *Id*. at 7:26–34.

Regarding recitation in claim 1 of the "register circuit" supplying "copies of the incoming command and address signals" having the "same frequency" as the incoming command and address signals (Ex. 1001, 7:21–25), Petitioner points to Lee's teachings relating to register 45 temporarily storing command and address signals and then supplying copies of these signals to chips 39 under control of the WCLK signal. Pet. 46–48 (citing Ex. 1008, 7:35–41, 11:29–37, Fig. 4; Ex. 1003, Fig. 1; Ex. 1011 ¶¶ 78–80). Dr. Subramanian testifies that copies of the command and address signals are provided to exemplary memory devices on the left and exemplary memory devices on the right such that the supplied command and address signals have the same frequency as the

incoming ones. Ex. 1011 ¶¶ 79–80 (citing e.g, Ex. 1008, 7:35–42, 11:29–37, Fig. 4). We credit Dr. Subramanian's testimony (*id.*) because it is consistent with Lee's teachings illustrated in Figure 4 of command and address signals, depicted as "C/A" (shown in red annotations in Figure 4 above) being supplied to memory devices to the left and memory devices to the right. Patent Owner does not dispute Petitioner's showing, except with respect to the recitation of "to generate a plurality of copies," which we discuss below.

Claim 1, additionally, recites a register circuit arranged on the memory module in a common chip packing with the clock regeneration circuit and configured to receive copies of the clock signal from the clock regeneration circuit. Ex. 1001, 7:14–18. Petitioner points to Lee's teachings relating to module 27, comprising register 45 and PLL 41. Pet. 44–45 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 74–76). Consistent with Petitioner's contentions (*id.*), Lee teaches that memory module 27 may be implemented as a DIMM (Ex. 1008, 6:6–21, 7:26–27) and that memory module 27 includes register 45 and PLL 41 (*id.* at Fig. 4). Patent Owner does not dispute that Lee teaches a register circuit arranged on the memory module. PO Resp. 43–56.

b. Patent Owner's Contentions—Claim 1

We turn now to Patent Owner's contentions. Patent Owner makes three arguments regarding obviousness of claim 1 over Lee as follows: (1) Lee does not teach a copy of the clock having the same frequency going to the register circuit (PO Resp. 43–47); (2) Lee does not teach a register circuit and clock

circuit in a common chip packing (id. at 47–52); and (3) Lee does not teach a plurality of copies of the command and address signals (id. at 52–56). Lee shows a "WCLK/2" input to register 45 and "WCLK/2" is "a ***factor of two*** different from that of the incoming clock signal WCLK," Lee fails to teach that the one of the copies of the clock signal received by the register circuit has the same frequency as the incoming clock signal. PO Resp. 44–46.

Patent Owner's contention is premised on its narrow interpretation of claim 1 requiring that the "one of the copies of the incoming clock signal" that the register circuit is "configured to receive" has a same frequency as the incoming clock signal. As we discussed *supra* Section II.C.1, we reject Patent Owner's construction as inconsistent with the recitations in claim 1, in which "having a same frequency" modifies only those copies of the incoming clock signal that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory chips." Additionally, we are not persuaded that Patent Owner's construction is mandated by the embodiments of the '150 Patent Specification, which instead describe multiple copies sent to multiple branches or chip-groups. Lee's teaching relied upon by Petitioner (Pet. 45) is similar to the description in the '150 Patent Specification encompassed by claim 1 as in both cases copies of signals are made to supply copies to multiple branches or groups of semiconductor chips. *Compare* Ex. 1001, 2:57–59, 3:61–64, 5:67–6:6 *with* Ex. 1008, Fig. 4.

Furthermore, Petitioner presents persuasive contentions and evidence that claim 1 is obvious over Lee even under Patent Owner's proposed

interpretation. Pet. 45–48 (citing e.g., Ex. 1008, 7:35–41, Fig. 4; Ex. 1011 ¶¶ 77–80). For instance, Dr. Subramanian testifies that Lee teaches regenerating a local clock signal to control capture of the command and address signals. Ex. 1011 ¶¶ 77, 80 (citing Ex. 1008, 7:35–42, 11:29–37, Fig. 4). We credit Dr. Subramanian's testimony as it is consistent with the evidence cited therein. For instance, Lee teaches "regenerating an additional data write clock signal *from said received data write clock signal*, and using said additional regenerated data write clock signal to control the capture of command and address data within said register." Ex. 1008, 11:29–37. Importantly, as we noted in the Institution Decision (Dec. 27–28), Lee teaches that the frequency of that additional data write clock signal may be at a frequency of "X/N where X is the frequency of said received data write clock signal and N is an integer" (*id.* at 11:38–41). We further noted with respect to the last of these that because "1" is an integer, when "N" is "1" the same frequency is used.

Patent Owner relies upon claim 31 of Lee, which recites "the frequency of said additional data write clock signal is at a frequency of X/N where X is the frequency of said received data write clock signal and N is an integer." PO Resp. 47. Patent Owner, however, does not respond to our analysis in the Institution Decision regarding when "N" is "1" ("an integer") the same frequency is used. *Id.* Instead, Patent Owner asserts without explanation that this teaching "helps confirm that WCLK/2 and WCLK of Lee's Figure 4 are not the same frequency." *Id.*

Patent Owner's conclusory attorney argument is

unavailing. We find that Lee's disclosure that the frequency of the additional data write clock signal may be at a frequency of "X/N where X is the frequency of said received data write clock signal and N is an integer" (*id.* at 11:29–41) teaches or at least suggests receipt by the register of a copy of the incoming clock signal from the clock regeneration circuit, as recited in claim 1, that has the same frequency as the incoming clock signal (i.e., when "N" equals "1" (an integer)).

Additionally, we are persuaded by Petitioner's contentions (Pet. 45–48 (citing e.g., Ex. 1008, 7:35–41, 11:29–37, Fig. 4; Ex. 1011 ¶¶ 77–80)) and credit Dr. Subramanian's testimony that Lee teaches that register 45 is configured to receive a regenerated clock signal so as "to control capture of the command and address signals on the command address (C/A) signal lines 15." Ex. 1008, 7:35–41. Lee's register 45 is configured to receive the regenerated local WCLK signal from PLL 41 e.g., via one or more signal lines to clock in the command and address data. *Id.* at 7:35–41, Fig. 4. Such a regenerated local WCLK signal may include a clock signal having the same frequency as the incoming clock signal. *See, e.g., id.* at 7:35–41, 11:29–41. Thus, even assuming Patent Owner is correct that the recited "one of the copies of the incoming clock signal" must have the same frequency as the incoming clock signal and that Lee's WCLK/2 operates at half the frequency of WCLK, Lee's register 45 would nevertheless still be "configured to receive one of the copies of the incoming clock signal" because receiving the full frequency signal would not require register 45 to be "configured" any differently than as taught in Lee.

Reply 16–17.

Furthermore, Dr. Subramanian testifies that the number of buses or branches exiting register 45 is a "design choice" among a number of limited number of alternatives. *See, e.g.*, Ex. 1011 ¶ 79. We credit Dr. Subramanian's testimony as it is consistent with the evidence cited therein, including Lee's teachings discussed above. Ex. 1008, 7:35–41, 11:29–41, Fig. 4. We also find that Dr. Subramanian's testimony regarding why one having ordinary skill in the art would have modified Lee's teachings, for example, such that two buses are used to deliver two signals (rather than a single bus that branches into two pieces), provides sufficient articulated reasoning with rational underpinning to support the legal conclusion of obviousness. Ex. 1011 ¶ 79 ("One of ordinary skill in the art would have been motivated to use a known dual bus design at least to reduce the drive strength per bus needed.")

Patent Owner relies on Dr. Bernstein's testimony only as evidence supporting that the WCLK/2 signal has a different frequency from the WCLK signal, i.e., different by a factor of two. PO Resp. 43–47 (citing Ex. 2019 ¶ 105). However, even crediting Dr. Bernstein's testimony, we remain persuaded by Petitioner's contentions and evidence because Patent Owner's contentions are not commensurate with the scope of the claim. We further are persuaded by Petitioner's contentions and evidence, even under Patent Owner's proposed construction, because we find that other disclosures of Lee teach or suggest the recitation, as set forth immediately above. Ex. 1008, 7:35–41, 11:29–41; Ex. 1011 ¶¶ 79, 80.

Patent Owner also contends "[b]oth Petitioner and Patent Owner agree that . . . copies of the incoming clock signal cannot operate at multiples of the frequency of the incoming clock signal." PO Resp. 45. Patent Owner further contends "[t]hus, it is undisputed that in the invention, copies of the incoming clock signal must have the same frequency as the incoming clock signal." *Id*. Petitioner, however, has shown that Lee's copies of the incoming clock signal, i.e., the copies generated and supplied to the memory chips, have the same frequency as the incoming clock signal. For instance, as discussed above with respect to annotated Figure 4, we credit Dr. Subramanian's testimony as it is consistent with the evidence cited therein that Lee teaches that PLL 41 generates copies of incoming clock signal, namely WCLK 0–8, and supplies those copies to memory chips 39 and that each of the copies have the same frequency as input clock WCLK. Ex. 1011 ¶¶ 72, 73 (citing Ex. 1008, 6:51–55, Fig. 4).

Patent Owner's dispute (PO Resp. 43–47) pertains to only the clock signal received by register 45 that is set to provide a copy of the signals to the three exemplary memory devices on the left and a copy of the signals to the exemplary memory devices on the right. Ex. 1011 ¶ 79. To the extent that Patent Owner argues that Lee is not enabling, such argument is misplaced because there is a rebuttable presumption that the disclosure in a prior art patent, as here, is enabled. *See Amgen Inc. v. Hoechst Marion Roussel, Inc*., 314 F.3d 1313, 1355 (Fed. Cir. 2003); *see also In re Antor Media Corp*., 689 F.3d 1282, 1287−88 (Fed. Cir. 2012) (holding that prior art publications and patents are presumed to be

enabled).

We turn to Patent Owner's second contention that Lee does not teach a register circuit and clock signal regeneration circuit in a common chip packing (PO Resp. 47–52). Relying on the testimony of Dr. Subramanian, Petitioner contends that it would have been obvious to one of ordinarily skill in the art to include the register (Register 45) and the clock signal regeneration circuit (PLL 41) in a single chip packing and integrated on one chip. Pet. 44–45, 48 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 74–76, 82). As indicated above, Patent Owner does not dispute (PO Resp. 43–56) that Lee teaches that the register circuit is arranged on the memory module with the clock regeneration circuit. Ex. 1008, 7:26–27 ("FIG. 4 illustrates in greater detail a memory subsystem 27, which as noted, may be a DIMM [dual in-line memory module] memory device."), Fig. 4 (illustrating memory module 27 having "REGISTER" 45 and "PLL" 41).

Patent Owner contends that the Petition's assertion is insufficiently supported because Dr. Subramanian's testimony is based on vague statements in Lee that do not suggest putting Lee's register and PLL in a common chip packaging. PO Resp. 47–48. Dr. Subramanian testifies that it would have been obvious to include the register (Register 45) and the clock signal regeneration circuit (PLL 41) in a common chip packing and integrated on a common chip because Lee teaches flexible packaging options, including the option to package constituent components together. Ex. 1011 ¶¶ 75, 82 (citing Ex. 1008, 8:25–28). We credit Dr. Subramanian's testimony because it is consistent with Lee's

teaching of "a one-chip memory controller or a chip set or may be a separate processor or part of a processor." Ex. 1008, 8:25–28. Patent Owner contends that Lee's teaching pertains to "other elements." PO Resp. 48. However, we credit Dr. Subramanian's testimony because consistent with his explanation (Ex. 1011 ¶¶ 75, 82), Lee's teachings pertain to memory controller 11, which like Register 45 and PLL 41 provides control for the memory devices. Ex. 1008, 8:25–28.

Patent Owner contends "[i]n the alternative" Petitioner asserts that "this limitation is a mere 'design choice[] for packaging these components,'" but merely stating that a particular placement of an element is a design choice does not make it obvious. PO Resp. 48-49 (citing *Cutsforth, Inc. v. Motivepower, Inc.*, 636 Fed. App'x 575, 578 (Fed. Cir. 2016) (nonprecedential)). In the instant proceeding, contrary to Patent Owner's contention, Petitioner's obviousness contention (Pet. 41–45) does not involve a rearrangement of parts. Patent Owner also contends an "unnumbered possibilities negate motivation to pick any particular possibility." PO Resp. 49 (citing *Insite Vision Inc. v. Sandoz, Inc.*, 783 F.3d 853, 860–61) (Fed. Cir. 2015)). We, however, credit Dr. Subramanian's testimony, for example, because he points to Lee's teachings regarding "one-chip memory" or "a chip set" as evidence supporting his testimony that these two design choices (i.e., packaged either together or separately) would have been known alternatives to a person of ordinary skill in the art. *Id*. at 8:26–27 (cited in Ex. 1011 ¶ 75).

Patent Owner also disputes Petitioner's design choice contentions on the basis that the common

packaging was an unexpected solution to stated problems in the '150 Patent Specification. PO Resp. 50 (citing Ex. 1001, 2:47–67, 3:1–29). Patent Owner further argues its contentions are supported by extrinsic evidence showing that the register and PLL "were not combined in a common chip until DDR3 RDIMMs" and the earlier generation DDR2 RDIMM used two discrete chips. PO Resp. 50–52 (citing Ex. 2019 ¶¶ 120–22; Ex. 2029; Ex. 2031, 2).

Upon consideration of the parties' contentions and evidence, we are persuaded by Petitioner's contentions and we credit Dr. Subramanian's testimony as consistent with the evidence of record. Dr. Subramanian testifies it would have been obvious to consolidate register 45 and PLL 41 because "the industry trend both at the time the 150 was filed and now is to consolidate circuits within fewer chip packages, as this reduces costs and facilitates manufacturing of systems with the packages." Ex. 1011 ¶ 76. Dr. Bernstein testifies "there was much discussion around moving the register and PLL to a single chip when DDR3 was developed in the late 2000s." Ex. 2019 ¶ 121 (citing Ex. 2032, 2); see also Ex. 2032, 2 ("DDR2 employs at least one register and a PLL instead of two separate components; DDR3 employs a single monolithic-IC chip, which integrates the register and PLL.")

Dr. Bernstein's testimony is consistent with Dr. Subramanian's testimony that the industry trend was to integrate the register and PLL. *Compare* Ex. 2019 ¶ 121 *with* Ex. 1011 ¶ 76. The dispute pertains to the timing of this trend. Ex. 1011 ¶ 76; Ex. 2019 ¶ 121. Dr. Bernstein's testimony that "there was much discussion around moving the register and PLL to a

single chip when DDR3 was developed in the late 2000s" identifies as support an article entitled "Evolving to DDR technology" dated May 28, 2009. Ex. 2019 ¶ 121 (citing Ex. 2032). That article refers to "[t]he *latest* DDR3-memory standard, JEDEC JESD79-3A" and also refers to a "DDR3 SDRAM Specification" dated September 2007. Ex. 2032, 1, 5. The references to the standards "3A" and "3B" may be indicative that these are not the first of the DDR3 standards. *Id*. Dr. Bernstein also testifies "DDR2 RDIMMs had their PLLs and registers on separate chips on the module and this did not change until years after the '150 Patent." Ex. 2019 ¶ 120 (citing Exs. 2029–2031). This testimony of Dr. Bernstein and evidence cited therein (*id*.) pertain to commercial availability of DDR systems, not when it would have been obvious to one of ordinary skill in the art to integrate a PLL and register on a common chip and in a common chip packaging and the testimony is vague with respect to "years after" (*id*.).

Upon consideration of the parties' contentions regarding this limitation and the evidence of record, we credit Dr. Subramanian's testimony regarding the timing and give it substantial weight because Dr. Subramanian's testimony that it would have been obvious to one of ordinary skill in the art to consolidate the register in a common chip packing and integrated on a common chip with the clock regeneration circuit is consistent with the evidence of record. Ex. 1011 ¶ 76. In comparison, we give Dr. Bernstein's testimony regarding the timing little to no weight because it is inconsistent with the evidence of record. Ex. 2019 ¶ 121. Lee, for example, describes that memory controller 11, which has PLL

13 (Ex. 1008, Fig. 1), "can be a one-chip memory controller or a chip set" (*id*. at 8:24–26). As an additional example, the '150 Patent Specification describes "DDR3" in the Background and indicates that DDR technology was known, i.e., "*[p]resent* memory systems (DDR1; DDR2; DDR3)." Ex. 1001, 1:20 (emphases added); *see also id*. at 1:33–35 (describing a consideration for "successor technologies of the DDR3 system, for example for DDR4.").[7] This is consistent with Dr. Subramanian's testimony and not Dr. Bernstein's testimony because the evidence supports Dr. Subramanian's testimony (Ex. 1011 ¶ 76) that the industry trend at the time the '150 Patent was filed was to consolidate circuits within fewer chips.

We turn to the third of Patent Owner's contentions, i.e., that Lee does not teach a plurality of copies of the command and address signals. PO Resp. 52–56. Patent Owner contends Lee does not

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[7] Patent Owner provides additional contentions (PO Resp. 56–58) for dependent claim 5, which recites the further recitation that "the clock signal regeneration circuit and the register circuit are integrated on a common chip" (Ex. 1001, 7:36–38), which we have considered in full, as we discuss below. Although not necessary for our determination, contrary to those Patent Owner contentions (PO Resp. 56–58), as further extrinsic evidence that it was known to integrate on a common chip a clock signal and an address and command register, consistent with Petitioner's contentions (Pet. 26), Dodd teaches clock circuit 300 and clock driver 310 embedded in ADDR/CMD buffer 122. Ex. 1003, 3:51–65, 5:57–6:11, Fig. 3; Ex. 1011 ¶ 19, 44, 79, 82. Also, consistent with Petitioner's contentions (Pet. 25) Dodd teaches that "a PLL is utilized to implement the clock circuit 300 for performing synchronization" (Ex. 1003, 5:6–32, Fig. 4) and ADDR/CMD 122 is a buffer or register (*id*. at 2:39–3:3).

disclose making multiple copies of the command and address signals because Figure 4 illustrates "multiple lines labeled C/A coming into register **45** and only one line labeled C/A coming out of it." *Id*. at 53.

We, however, are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony that making copies of the incoming command and address signals would have been obvious over Lee's teachings because Petitioner's contentions and Dr. Subramanian's testimony are consistent with the evidence cited therein, including Lee's teachings. Pet. 46–48 (citing e.g., Ex. 1011 ¶¶ 78–80). For instance, contrary to Patent Owner's contention that "one line" comes out of register 45 (PO Resp. 53), consistent with Petitioner's contentions (*see, e.g.*, Pet. 46–47; Reply 19), Lee illustrates hash marks on the line exiting register 45, which indicate that multiple lines, e.g., a bus, exiting register 45. Ex. 1008, Fig. 4.

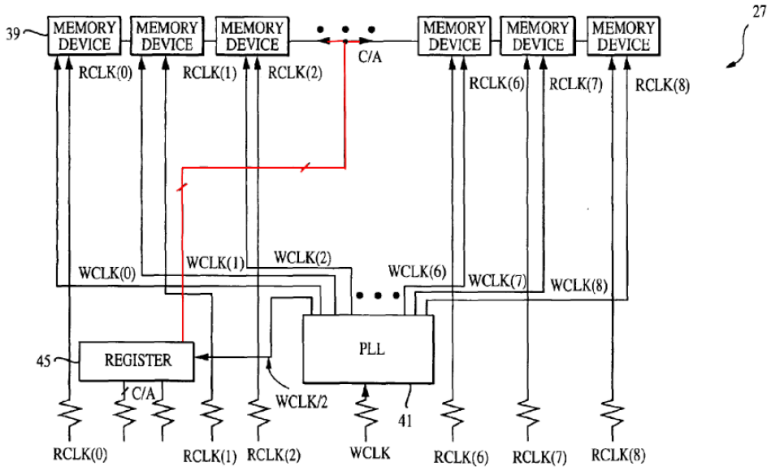

FIG. 4

Figure 4 illustrates Memory Subsystem 27 with Annotations by the Board

Figure 4 of Lee reproduced above has been annotated in red to show the line with hash marks leaving register 45 carrying command and address signals. Dr. Subramanian testifies that it would have been obvious in view of Lee's teaching, for example, to supply multiple copies of the incoming command and address signals. Ex. 1011 ¶ 79. We credit Dr. Subramanian's testimony because it is consistent with Lee's teaching of command and address signals being sent from register 45 to multiple memory devices 39, including the memory devices on the left and the memory devices on the right, as well as other evidence cited. See, e.g., Ex. 1008, Fig. 4; Ex. 1003, Fig. 1 (illustrating two buses carrying command and address signals). Supplying command and address signals to two groups of memory devices, e.g., memory devices on the left and memory devices on the right is similar to embodiments described in the '150 Patent Specification, which for the reasons discussed above *supra* in Section II.C.1, we determine are encompassed in the scope of claim 1. *Compare* Ex. 1001, 2:57–59 (providing "several" copies "to *several DRAM branches or channels*") *with* Ex. 1008, Fig. 4; *see also* Ex. 1001, 5:57–6:9 (describing providing command and address signals to "two semiconductor memory chip groups."). Furthermore, Petitioner's contentions also are consistent with the deposition testimony of Dr. Bernstein regarding the hash marks illustrated in Figure 4 of Lee "I think it's generally understood that when we see a hash it's representing many lines in parallel representing . . .

[a] parallel set of connections." Ex. 1020, 111:17–24.

Patent Owner also argues that a branch does not make a copy. PO Resp 54 (citing Ex. 2019 ¶¶ 67, 113; Ex. 2018, 115:22–23). Patent Owner further argues that Lee shows "that the outgoing C/A signals are ***branched*** off the incoming signals." *Id.* Patent Owner's contentions, however, do not apply to Petitioner's argument and Dr. Subramanian's testimony that it would have been obvious in view of Lee's teachings for copies to be made by register 45, e.g., by using a dual-bus architecture. Ex. 1011 ¶¶ 79, 80 (citing, e.g., Ex. 1008, Fig. 4; Ex. 1003, Fig. 1). Additionally, to the extent that Patent Owner's contentions imply that branching results in fewer signals, the contentions are not consistent with the evidence of record. For instance, Dr. Subramanian testifies: "A branch does not make a copy. It provides the same signal to everything." Ex. 2018, 115:22–24. Dr. Bernstein's testimony regarding the distinction between branching and copying pertains to electrical characteristics of the signal. *See, e.g.*, Ex. 2019 ¶ 113. Furthermore, Lee teaches multiple memory devices 39 (six exemplary devices illustrated) receiving command and address signals. Ex. 1008, Fig. 4.

Relying on the testimony of Dr. Bernstein, Patent Owner, additionally, argues that "'[i]n contrast to the multiple WCLK signals ("WCLK(0)–WCLK(8)") that emanate from the PLL 41, this one C/A line in Lee would clearly suggest to a POSITA that no copies are made at the Register 45." PO Resp. 54 (citing Ex. 2019 ¶ 111). However, the "one C/A line" (id.) is the line with hash marks that Dr. Bernstein acknowledged represents "many lines in parallel" (Ex. 1020, 111:17–24), and this contention

does not pertain to Petitioner's contentions and Dr. Subramanian's testimony regarding obviousness. Additionally, register 45 need not have eight lines exiting it to teach "a plurality of copies" recited in claim 1. Claim 9, which depends from claim 1 and is not contested by Patent Owner, further recites "wherein the clock signal regeneration circuit and the register circuit respectively generate *two copies* of the clock signal and the *command and address signals* for distribution to the memory chips." Ex. 1001, 8:1–5 (emphases added). Additionally, Lee's teaching is similar to embodiments described in the '150 Patent Specification, which for the reasons discussed above supra in Section II.C.1, are encompassed in the scope of claim 1, describing only two lines exiting. *Compare* Ex. 1001, 5:57–6:9 (describing providing command and address signals to "two semiconductor memory chip groups") *with* Ex. 1008, Fig. 4.

Again, relying on the testimony of Dr. Bernstein, Patent Owner argues because Lee has "multiple C/A signals entering the register," Lee does not teach copying the signals and a person having ordinary skill in the art would not have a reason to modify Lee to add this limitation. PO Resp. 54–56 (citing *e.g.*, Ex. 2019 ¶¶ 112–16). Dr. Bernstein testifies "Lee has more than one C/A line entering register 45," which is "what the '150 Patent was designed to avoid." Ex. 2019 ¶ 115–16 (citing Ex. 1001, 1:29–32). However, the '150 Patent Specification illustrates multiple incoming command address ("CA") signal lines, again depicting hash marks. Ex. 1001, Figs. 1-5; *see also id*. at 5:30–38 ("as was the case in the first embodiment . . . command and address *signals* CA

that are supplied to the module 100 via *CA lines* 71") (emphases added), 5:38–41 ("In the second embodiment . . . the differential command and address *signals* CA are supplied via the input CA *lines* 71") (emphases added), 5:62–66 ("the invention proposes to arrange . . . a clock signal regeneration circuit and a register circuit . . . and to connect them to *bus signal lines 61, 71* supplying the command and address *signals*") (emphases added). Lee's teaching of a bus (the line to the left with the hash mark) and a single line (to the right) providing incoming signals to register 45 is substantially the same as the embodiments depicted in the '150 Patent Specification of using a bus to receive command and address signals, for example, line 71 with hash marks denoted "CA signal lines," for example in Figure 2. *Compare* Ex. 1008, Fig. 4 *with* Ex. 1001, Figs. 1–5.

Additionally, Patent Owner's contentions and Dr. Bernstein's testimony (PO Resp. 56; Ex. 2019 ¶¶ 115–16) pertain to a different modification than that set forth in Petitioner's contentions and Dr. Subramanian's testimony (Pet. 46–47; Ex. 1011 ¶ 79). In particular, Patent Owner's contentions and Dr. Bernstein's testimony (PO Resp. 56; Ex. 2019 ¶¶ 115–16) assume an "increased number of pins" for incoming command/address signals, whereas Petitioner's contentions and Dr. Subramanian's testimony pertain to generating copies, rather than receiving the copies (Pet. 46–47; Ex. 1011 ¶ 79).

Furthermore, even if multiple copies were received, Patent Owner's contentions and Dr. Bernstein's testimony (PO Resp. 54–56 (citing *e.g.*, Ex. 2019 ¶¶ 112–16) are not commensurate with the

scope of claim 1, which does not prohibit more than one incoming line and recites that the register circuit is "configured to temporarily store the incoming command and address *signals*." Ex. 1001, 7:18–20. Claim 1 also is directed to a memory module "comprising" the various elements recited. *Id.* at 7:2. The term "comprising" is a term of art used in claim language, which means that the named elements are essential, but other elements also may be included to constitute additional components within the scope of the claim. *See Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997).

Upon consideration of Dr. Subramanian's testimony that it would have been obvious over Lee's teachings "to generate a plurality of copies of the incoming command and address signals," by register 45, for example, by using two buses to provide copies of the incoming command and address signals to memory devices 39 (one bus for devices on the left and one bus for devices on the right) (Ex. 1011 ¶ 78–80) and Dr. Bernstein's testimony (Ex. 2019 ¶¶ 110–16), we credit and give substantial weight to Dr. Subramanian's testimony because we find it consistent with the teachings of the art cited therein. In contrast, we give Dr. Bernstein's testimony little or no weight. Ex. 2019 ¶¶ 110–16. Regarding the evidence of record, Lee, for instance, teaches that register 45 "capture[s]" the incoming command and address signals and "clocks in the command and address data." Ex. 1008, 7:34–41. Patent Owner does not dispute that Lee's register 45 temporarily stores the incoming command and address signals. PO Resp. 43–56. Lee's Figure 4 also illustrates register 45 then providing copies of the incoming command

and address signals to memory devices 39 via the line with hash marks . Ex. 1008, Fig. 4; Ex. 1011 ¶ 79. Furthermore, Figure 4 of Lee also includes a "C/A" label at the top of Figure 4 illustrating providing command and address signals to three memory devices on the left-hand side and three memory devices on the right-hand side. *Id*. at Fig. 4. We are persuaded that it would have been obvious in view of these teachings, for example, to use the dual bus design with two copies leaving register 45, as testified by Dr. Subramanian. Ex. 1011 ¶¶ 79, 80; *see also* Ex. 1020, 111:17–24 (Dr. Bernstein testifies "I think it's generally understood that when we see a hash it's representing many lines in parallel representing . . . [a] parallel set of connections.") Additionally, Lee is directed to "a clocking system and method for effecting high speed data transfers" (*id*. at 1:10–12) and specifically teaches providing command and address (C/A) signals to a plurality of memory storage devices via a register (*id*. at 4:1–14, 7:34–41, 11:4–41, Fig. 4).

Patent Owner's argument fails to recognize that "[w]hat a prior art reference discloses or teaches is determined from the perspective of one of ordinary skill in the art." *Sundance, Inc. v. DeMonte Fabricating Ltd*., 550 F.3d 1356, 1361 n.3 (Fed. Cir. 2008). A prior art reference must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994); *see also; DeGeorge v. Bernier*, 768 F.2d 1318, 1323 (Fed. Cir. 1985) (superseded on other grounds by statute, Patent Law Amendments Act of 1984, 35 U.S.C. §§ 135, 141–46) (holding that a reference "need not, however, explain every detail

since [it] is speaking to those skilled in the art"); *In re Preda*, 401 F.2d 825, 826 (CCPA 1968) (explaining that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom").

We further are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony that it also would have been obvious to one having ordinary skill in the art to modify Lee's teachings to use two buses and deliver the plurality of copies of the command and address signals over those buses because sufficient reason is given for this modification. Pet. 46–48 (citing *e.g.*, Ex. 1011 ¶¶ 78–80). For instance, Dr. Subramanian testifies "one of ordinary skill in the art would have understood that the choice between using a single bus that branches into two pieces to deliver two signals or to use two buses was a simple design choice." Ex. 1011 ¶ 79 (citing *e.g.*, Ex. 1003, Fig. 1). We credit Dr. Subramanian's testimony because he testifies that using two buses was a design choice among a number of limited number of alternatives, e.g., using a single bus that branches or two buses. We also credit Dr. Subramanian's testimony that using two buses was a design choice that would have been known because it is consistent with the evidence cited therein including, for example, Figure 1 of Dodd (Ex. 1003), which illustrates a single input into ADDR/CMD buffer 122 and two buses (denoted with hash marks) exiting ADDR/CMD buffer 122. Ex. 1003, Fig. 1. The buses exiting ADDR/CMD buffer 122 carry copies of the incoming address and

command signals, the top bus carrying signals to memory devices 130 and 140 and the bottom bus carrying signals to memory devices 135 and 145. *Id*. We find that Dr. Subramanian's testimony also provides a motivation to use the dual bus design. *See, e.g.*,Ex. 1011 ¶ 79 ("One of ordinary skill in the art would have been motivated to use a known dual bus design at least to reduce the drive strength per bus needed.") Accordingly, we find that Dr. Subramanian's testimony provides sufficient articulated reasoning with rational underpinning to support the legal conclusion of obviousness.

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 1 are obvious over Lee.

c. Conclusion—Claim 1

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 1 is unpatentable under § 103(a) as obvious over Lee.

4. Discussion of Claims 2, 5, 6, and 8–10

Each of claims 2, 5, 6, and 8–10 depends directly from independent claim 1. We have reviewed Petitioner's showing (Pet. 48–52) with respect to dependent claims 2, 5, 6, and 8–10 and the teachings of Lee.

a. Claim 2

Claim 2 recites "wherein the clock signal regeneration circuit comprises a phase locked loop (PLL) circuit." Ex. 1001, 7:26–28. We are persuaded

by Petitioner's contentions (Pet. 48) because Lee teaches that the clock regeneration circuit is PLL 41. *See, e.g.*, Ex. 1008, Fig. 4. Patent Owner does not contest separately Petitioner's showing for claim 2. Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 2 are obvious over Lee.

b. Claim 5

Claim 5 recites "wherein the clock signal regeneration circuit and the register circuit are integrated on a common chip in the common chip packing." Ex. 1001, 7:36–38. Petitioner relies on its contentions for claim 1. Pet. 48; Reply 20. Patent Owner also relies on its contentions for claim 1, but, additionally, contends that "it is far from straightforward" to integrate on a common chip PLL 41, which is an analog device and register 45, which is a digital device. PO Resp. 57–58 (citing *e.g.*, Ex. 1003, 5:40–43; Ex. 2019 ¶¶ 118, 119, 122). Dr. Bernstein testifies that "[i]t is difficult and expensive to integrate analog and digital systems on a single chip" relying on Dodd's teachings. Ex. 2019 ¶ 118 (citing Ex. 1003, 5:40–43). Although Dodd indicates "in a digital system such as memories, a PLL having analog characteristics may introduce analog design complications in a mainly digital design" (Ex. 1003, 5:40–43), Dodd also teaches "[a]s compared to using a DLL, the advantages of using a PLL, is that the PLL is more accurate" (*id.* at 5:36–37). Additionally, consistent with Petitioner's contentions (Pet. 26), Dodd teaches an embodiment in which clock circuit 300 and clock driver 310 are embedded in

ADDR/CMD buffer 122. Ex. 1003, 3:51–65, 5:57–6:11, Fig. 3; Ex. 1011 ¶ 19, 44, 79, 82. Also, consistent with Petitioner's contentions (Pet. 25) Dodd teaches that "a PLL is utilized to implement the clock circuit 300 for performing synchronization" (Ex. 1003, 5:6–32, Fig. 4) and ADDR/CMD 122 is a buffer or register (*id*. at 2:39–3:3). Dr. Bernstein also testifies regarding other complexities (*see, e.g*., Ex. 2019 ¶ 119), but as Dr. Bernstein testifies, these complexities were overcome (*id*. ¶¶ 120, 121).

Upon consideration of all Patent Owner's contentions, including those presented for both claims 1 and 5, we are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony for the same reasons discussed *supra* Section II.D.3 with respect to claim 1. Indeed, throughout our discussion of claim 1, we referred to "common chip packing" in connection with "integrated on a common chip" as both parties' contentions for claim 1 and "common chip packing" pertain to whether the clock signal regeneration circuit and the register circuit are both in "common chip packing" and also "integrated on a common chip." We, again, note that our finding that Petitioner's contentions are persuasive and our crediting of Dr. Subramanian's testimony is based, for example, on Lee's express teaching of employing on "a one-chip memory or a chip set" memory controller 11, having a PLL and which communicates digital data to and from memory devices 39. Ex. 1008, 8:24–29, Fig. 1.

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 5 are

obvious over Lee.

c. Claim 6

Claim 6 recites "wherein the common chip packing is arranged essentially at a central position on the memory module." Ex. 1001, 7:39–41. Petitioner contends it would have been obvious to one having ordinary skill in the art to arrange the common chip packing at a central position on the memory module. Pet. 48–49 (citing *e.g.*, Ex. 1011 ¶¶ 83–84). Dr. Subramanian testifies that Lee teaches locating the common chip packaging in essentially a central position on the memory module because Lee discloses PLL 41 located in a central position. Ex. 1011 ¶ 83. Dr. Subramanian also testifies one of ordinary skill in the art would have known that the PLL and register circuit should be placed in a central location and would have had reasons to do so including that such placement would have been known to simplify the design. *Id.* ¶¶ 83, 84 (citing Ex. 1008, Fig. 4; Ex. 1010, Fig. 2).

For claim 6, relying on the testimony of Dr. Bernstein, Patent Owner contends that Lee's Figure 4 does not illustrate a physical arrangement because it is a circuit diagram and "so the same reasoning discussed with respect to Dodd in Section IV.C, *supra*, also applies here to Lee." PO Resp. 60 (citing Ex. 2019 ¶ 124). In addition to testifying regarding Lee, Dr. Bernstein testifies "the statements I made in ¶¶ 89–97, *supra*, for Dodd are equally applicable to Lee." For the most part, Patent Owner's contentions and Dr. Bernstein's testimony regarding Dodd, however, apply particularly to Dodd and not to Lee. PO Resp. 29–39; Ex. 2019 ¶¶ 89–97. The Patent

Owner Response must include "a detailed explanation of the significance of the evidence." *See* 37 C.F.R. §§ 42.22, 42.23, 42.120. Such a detailed explanation is not provided. To the extent contentions or testimony are reasonably understood to apply to both Lee and Dodd, we provide a response. We decline, however, to try to ascertain what Patent Owner might have argued with respect to Lee.

We now turn to Patent Owner's contention and Dr. Bernstein's testimony that Lee's Figure 4 does not illustrate a physical arrangement because it is a circuit diagram. PO Resp. 60; Ex. 2019 ¶ 124. Dr. Bernstein testifies "Lee is a circuit diagram that shows how different circuit elements are connected, rather than a layout diagram that shows where the circuit elements are physically located on a module." Ex. 2019 ¶ 124. Dr. Bernstein testifies that Dr. Subramanian agrees. *Id*. ¶ 90 (citing Ex. 2018 129:24–130:2, 130:13–18). Dr. Bernstein testifies that his "conclusion" "is reinforced by the fact that the register **45** is located in the bottom left corner of the diagram." *Id*. ¶ 124. Dr. Bernstein also testifies "Petitioner also states that it would be obvious to place the register circuit and clock regeneration circuit at a central position of the memory module," but "Petitioner does not cite to any evidence in Lee to support this contention." Ex. 2019 ¶ 124 (citing Pet. 49).

Dr. Subramanian testifies

> Q. On what way is a circuit diagram is different from a layout diagram?
>
> A. The way a circuit diagram is drawn is

> intended to emphasize the electrical structure and essentially establish the electrical functional relationships between components. The way a layout is drawn, it's intended to emphasize the special structure. However, it turns out it is possible to go from one to the other and back. *So, in other words from a circuit diagram you can calculate a layout or generate a layout and from a layout you can back circuit what the circuit diagram is*. So they're essentially -- they contain similar information with different things emphasized.
>
> Q. How can you calculate a layout diagram from a circuit diagram?
>
> A. *If you have a circuit diagram you can generate a layout that would correspond to that circuit, which will specify the wiring, will specify the component placement, etcetera*. In fact, today a lot of that is automated and it has been automated for awhile.

Ex. 2018, 130:13–131:10 (emphases added). Additionally, Dr. Subramanian testifies that "in Figure 4 [of Lee], the PLL chip is disclosed to be located in a central position on the module." Ex. 1011 ¶ 83.

Upon consideration of Dr. Subramanian's testimony (*see, e.g.*, Ex. 1011 ¶¶ 83–84, Ex. 2018, 129:8–131:10) and Dr. Bernstein's testimony (*see, e.g.*, Ex. 2019 ¶¶ 90, 124), we credit Dr. Subramanian's testimony and give it substantial weight (*see, e.g.*, Ex. 1011 ¶¶ 83–84, Ex. 2018, 129:8–

131:10), whereas we give Dr. Bernstein's testimony (see, e.g., Ex. 2019 ¶¶ 90, 124) little to no weight because we find that Dr. Subramanian's testimony is consistent with the evidence cited therein. As an initial matter, we decline to discount Dr. Subramanian's testimony and the evidence that he relies on because the diagrams in the patents are not expressly identified as layout diagrams. It is well settled that things patent drawings show clearly are not to be disregarded. *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972).

Consistent with Dr. Subramanian's testimony (Ex. 1011 ¶ 83), Lee illustrates PLL 41 located in a central position in Figure 4. Dr. Subramanian also testifies one of ordinary skill in the art would have known that the PLL and register circuit should be placed in a central location and would have had reasons to do so including that such placement would have been known to simplify the design. *Id.* ¶¶ 83, 84 (citing Ex. 1008, Fig. 4; Ex. 1010, Fig. 2). Regarding Dr. Bernstein's testimony that "the register **45** is located *in the bottom left corner of the diagram*" (Ex. 2019 ¶ 124), consistent with Dr. Subramanian's testimony (Ex. 1011 ¶¶ 75, 76 82–84) we find that register 45 is placed to the left, and alongside, PLL 41, indicating that the two components should be located together, *e.g.*, side-by-side. Ex. 1008, Fig. 4.

Regarding Dr. Bernstein's testimony that "Petitioner also states that it would be obvious to place the register circuit and clock regeneration circuit at a central position of the memory module," but "Petitioner does not cite to any evidence in Lee to support this contention" (Ex. 2019 ¶ 124 (citing Pet.

49)), we are persuaded by Petitioner's contentions supported by Dr. Subramanian's testimony and the other evidence cited therein. Pet. 44–45, 48–49 (citing *e.g.*, Ex. 1008, Fig. 4; Ex. 1010, Fig. 2; Ex. 1011 ¶¶ 75–76, 82–84); Reply 20–21 (citing *e.g.*, Ex. 1008, Fig. 4; Ex. 1010, Fig. 2). For instance, the PLL 41 is shown in Figure 4 of Lee in an essentially central location similar to that illustrated in embodiments in the '150 Patent Specification. *Compare* Ex. 1008, Fig. 4 *with* Ex. 1001, Figs. 1, 3 (illustrating a placement near, but not exactly at the center). Additionally, we credit Dr. Subramanian's testimony (Ex. 1011 ¶¶ 75, 76 82–84), for example, because we find it is consistent with Lee's teaching that a control element such as register 45 and PLL 41 "can be a one-chip memory controller or a chip set, or may be a separate processor, or part of a processor" (Ex. 1008, 8:25–27) taken together with the illustration in Figure 4 of PLL 41 in a central location (*id*. at Fig. 4). Furthermore, although not necessary for our determination, we also credit Dr. Subramanian's testimony (Ex. 1011 ¶ 84), for example, because it is consistent with the illustration of register 210 and PLL 212 in an essentially central location in registered memory module 200 in Figure 2 of Exhibit 1010.[8]

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 6 are obvious over Lee.

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[8] Exhibit 1010 is U.S. Patent Application Publication 2004/0143773 A1 and was published July 22, 2004.

d. Claim 8

Claim 8 recites "wherein the bus signal lines of the command and address signals comprise a fly-by bus structure." Ex. 1001, 7:45–47. We are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony that Lee teaches the further recitation of claim 8 because Petitioner's contentions and Dr. Subramanian's testimony are consistent with the evidence cited therein. Pet. 50–51 (citing *e.g.*, Ex. 1008, Fig. 4; Ex. 1001, Fig. 5; Ex. 1011 ¶¶ 85–86). For instance, we find that Figure 4 of Lee illustrates address/command buses that fly by multiple memory devices. Ex. 1008, Fig. 4. Additionally, Figure 4's fly-by structure is similar to that shown in Figure 5 of the '150 Patent, which is described as being "a schematic layout view of the [ ] semiconductor memory module with fly-by bus structure with two copies of the clock signal and command address signal bus," (Ex. 1001, 4:23–26) which is encompassed in the scope of claim 8. *Compare* Ex. 1008, Fig. 4 *with* Ex. 1001, Fig. 5.

Patent Owner does not contest separately Petitioner's showing for claim 8. Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 8 are obvious over Lee.

e. Claim 9

Claim 9 recites "wherein the clock signal regeneration circuit and the register circuit respectively generate two copies of the clock signal and the command and address signals for distribution to the memory chips." Ex. 1001, 8:1–5.

We are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony for the same reasons discussed *supra* in Section II.D.3 with respect to claim 1. Pet. 51 (citing Ex. 1011 ¶ 87).

Patent Owner does not contest separately Petitioner's showing for claim 9. Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 9 are obvious over Lee.

f. Claim 10

Claim 10 recites "wherein the memory module comprises an RDIMM module." Ex. 1001, 8:6–7. As we discussed with respect to claim construction *supra* in Section II.C.2, we need not make a determination regarding the broadest reasonable interpretation of "RDIMM" because we are persuaded that Petitioner shows sufficiently that Lee teaches an "RDIMM" based on Patent Owner's proposed construction. Accordingly, for the purpose of this Decision, RDIMM means "registered dual in line memory module, which buffers control signals, but not data signals."

Relying on the testimony of Dr. Subramanian, Petitioner contends that Lee's memory subsystem 27 teaches an RDIMM. Pet. 52 (citing Ex. 1008, 7:25–27, Fig. 4; Ex. 1011 ¶ 88). Dr. Subramanian testifies that Lee discloses an R-DIMM because the DIMM (shown in Figure 4) includes register 45. Ex. 1011 ¶ 88.

Patent Owner contends "[t]he Petition[er] offers little explanation of how Lee supposedly meets this limitation." PO Resp. 61. Patent Owner further

contends "Figure 4 does not show—and Lee does not specify—whether or what, buffering occurs on the data lines so it is impossible to tell if it discloses a RDIMM or FB-DIMM." *Id*. at 62, n.11.

Patent Owner contends "Dr. Subramanian states that 'if there is a DIMM that provides buffering for control signals and also data signals,' then 'traditionally that would be an FBDIMM.'" PO Resp. 12, n. 2 (citing Ex. 2018, 16:20–25, 19:7–11). Dr. Subramanian, additionally, testifies that Lee discloses an R-DIMM. Ex. 1011 ¶ 88 (citing e.g., Ex. 1008, 7:25–27, Fig. 4). We credit Dr. Subramanian's testimony that Lee discloses an R-DIMM because, consistent with his testimony, Lee teaches that memory subsystem 27 "may be a DIMM [dual in-line memory module] device." Ex. 1008, 7:25–28; *see also id*. at 6:6–7 ("[E]ach of the memory subsystems 27 is constructed as a [ ] dual in-line memory module (DIMM.")). Additionally, according to Patent Owner, Dr. Subramanian agrees with Patent Owner's proposed construction. Furthermore, Figure 4 of Lee illustrates *only* Register 45, PLL 41, and memory devices 39, as well as clock and command and address signal lines, as discussed above in various previous sections. Ex. 1008, Fig. 4. Consistent with Patent Owner's proposed construction of "RDIMM" i.e., "registered dual in line memory module, which buffers control signals, but not data signals" (PO Resp. 61), Lee illustrates controlling capture of command and address signals without buffering data signals (Ex. 1008, 7:34–40, Fig. 4). Accordingly, we find that Petitioner has shown sufficiently that Lee teaches "wherein the memory module comprises an RDIMM module," recited in claim 10 and RDIMM

means "registered dual in line memory module, which buffers control signals, but not data signals."

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 10 are obvious over Lee.

g. Conclusion—Claims 2, 5, 6, and 8–10

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 2, 5, 6, and 8–10 are unpatentable under § 103(a) as obvious over Lee.

5. Discussion of claims 3 and 11

We next turn to dependent claims 3 and 11, each of which depends directly from independent claim 1. Petitioner asserts that the combination of Lee and Keith teaches all elements of claims 3 and 11 and provides a rationale for combining the teachings of Lee and Keeth. Pet. 52–54.

a. Claims 3 and 11

Claim 3 recites "wherein the incoming clock signal and the copies of the incoming clock signal are each supplied via differential clock signal lines." Claim 11 recites "wherein the memory chips comprise DDR-DRAM memories." Petitioner contends that differential signaling was well-known and points to Keeth's teachings of memory devices using differential signaling for clock signals in DDR DRAM devices. Pet. 52–54 (citing *e.g.*, Ex. 1016, 1:25–44; Ex. 1011 ¶¶ 89–91). Relying on the testimony of Dr. Subramanian, Petitioner asserts it

would have been obvious to one of ordinary skill in the art to have used differential signaling for the clocks signals and the command and address signals due to its more precise timing, higher speed capability, and greater signal/noise ratios and performance. *Id*. Again relying on the testimony of Dr. Subramanian, Petitioner also asserts that one of ordinary skill would have used differential signaling with Lee to increase the speed of the memory, increase its bandwidth, and to comply with industry standards and practice. *Id*.

We are persuaded that Petitioner has accounted sufficiently for the limitations of claims 3 and 11. Additionally, relying on the testimony of Dr. Subramanian, Petitioner has articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have modified Lee's system so as to apply Keeth's teachings of DDR DRAM devices and using differential signaling for clock signals. Pet. 52–54 (citing *e.g*., Ex. 1016, 1:25–44; Ex. 1011 ¶¶ 89–91).

We credit Dr. Subramanian's testimony that the combination of Lee and Keeth teach all limitations recited in claims 3 and 11 and we credit his testimony providing articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have modified Lee's system so as to apply Keeth's teachings of DDR DRAM devices and using differential signaling for clock signals because his testimony is consistent with the evidence cited therein. Ex. 1011 ¶¶ 89–91 (citing e.g., Ex. 1016, 1:25–44). For instance, Keeth teaches that DDR DRAM "transfers data at both the rising and falling edge of a clock signal," which is "unlike traditional

SDRAM, which transfers data only on the rising edge of a clock signal," thereby increasing the speed of the memory. Ex. 1016, 1:25–44. Keeth also teaches that such memory devices use "differential signaling for clock signals," for example, because differential signaling "reduces sensitivity to common mode voltages to enable the production of a stable internal timing reference," and provides "good signal integrity from which a balanced receive can be built that maintains good duty cycle performance internally." *Id.*

Patent Owner does not argue for the separate patentability of claims 3 and 11 with respect to this challenge. PO Resp. 43–62. Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claims 3 and 11 are obvious over Lee and Keeth.

b. Conclusion—Claims 3 and 11

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 3 and 11 are unpatentable under § 103(a) as obvious over Lee and Keeth.

E. Obviousness of Claims over Dodd alone or with Keeth

Petitioner contends claims 1, 2, 5, 6, and 8–10 are unpatentable under 35 U.S.C. § 103(a) as

obvious over Dodd.[9] Pet. 4, 18–39. Petitioner also contends claims 3 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Dodd and Keeth. *Id*. at 4, 39–41. In light of our unpatentability determinations based on Lee, we take no position on whether these same claims are also obvious over Dodd alone or with Keeth.

F. Patent Owner's Listing of Improper Reply Arguments and Evidence

Patent Owner filed a Listing of Improper Reply Arguments and Evidence (Paper 26) and Petitioner filed a Response (Paper 29). Patent Owner lists several portions of Petitioner's Reply and evidence allegedly beyond the scope of what can be considered appropriate for a reply. *See* Paper 26. We have considered Patent Owner's listing, but disagree that the cited portions of Petitioner's Reply and reply evidence are beyond the scope of what is appropriate for a reply. Replies are a vehicle for responding to arguments raised in a corresponding patent owner response. Petitioner's arguments and evidence that Patent Owner objects to are not beyond the proper scope of a reply because we find that they fairly respond to Patent Owner's arguments raised in Patent Owner's Response. *See Idemitsu Kosan Co., LTD. v. SFC Co. LTD*, 870 F.3d 1376, 1381 (Fed. Cir. 2017) ("This back-and-forth shows that what Idemitsu characterizes as an argument raised 'too late' is simply the by-product of one party necessarily getting the last word. If anything,

[9] Although claim 11 is listed in the section heading for this ground (Pet. 18), the analysis of claim 11 is found within only the next section (*id*. at 39–41).

Idemitsu is the party that first raised this issue, by arguing—at least implicitly—that Arkane teaches away from non-energy-gap combinations. SFC simply countered, as it was entitled to do.").

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has established by a preponderance of the evidence that claims 1, 2, 5, 6, and 8–10 of the '150 Patent are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee. Additionally, we determine that Petitioner has established by a preponderance of the evidence that claims 3 and 11 are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee and Keeth.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–3, 5, 6, and 8–11 of the '150 Patent have been shown to be unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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APPENDIX H

Trials@uspto.gov Paper 7
571-272-7822 Entered: February 15, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE
PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,
v.
POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01622
Patent 6,850,414 B2

Before SALLY C. MEDLEY, JEAN R. HOMERE, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314 and 37 C.F.R. § 42.108

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–8 ("the challenged claims") of U.S. Patent No. 6,850,414 (Ex. 1001, "the '414 patent"). Paper 2 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the '414 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1 and 5–8 of the '414 patent.

A. Related Proceedings

The '414 patent is involved in *Polaris Innovations Ltd. v. Kingston Tech. Co., Inc.*, Case No. 8:16-cv-300 (C.D. Cal.). Pet. 1; Paper 4, 1. Petitioner also has filed other petitions seeking inter partes review of related patents: Case IPR2016-01621 and Case IPR2016-01623.

B. The '414 patent

The '414 patent, titled "Electronic printed circuit board having a plurality of identically designed, housing-encapsulated semiconductor memories,"

issued February 1, 2005, from U.S. Patent Application No. 10/187,763. Ex. 1001 at [54], [45], [21].

The '414 patent generally relates to an electronic printed circuit board having a memory module comprised of identically designed semiconductor memories configured on the printed circuit board. *Id.* at Abstract. According to the '414 patent, "Printed circuit boards of this type are inserted into motherboards of personal computers or network computers and serve as the main memory." *Id.* at 1:21–23. Figures 1A and 1B are reproduced below.

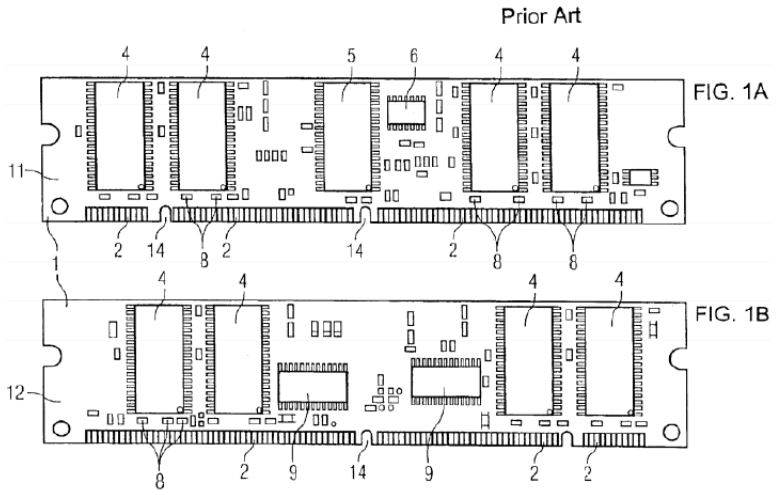

Figure 1A shows the front side of a conventional printed circuit board and Figure 1B shows the rear side of a conventional printed circuit board. *Id.* at 5:6–10. In a conventional arrangement, semiconductor memories 4 are arranged on the front and rear sides of the printed circuit board in the same orientation as error correction chip 5. *Id.* at 1:62–67. "In the case of this conventional arrangement . . . there is no more leeway for a

further reduction of the circuit board height (the height of the printed circuit board perpendicular to the contact strip)." *Id*. at 2:37–41. In network computers, however, "the printed circuit boards are inserted into compartment-type elements having a small height, for which reason the printed circuit boards themselves should also have only a small height." *Id*. at 1:23–27.

To address this problem, the '414 patent discloses an electronic printed circuit board in which the error correction chip remains oriented perpendicular to the contact strip but the other semiconductor memories are oriented parallel to the contact strip, such that it is "possible to reduce the height of the printed circuit board while enabling the rectangular housing to keep the same physical form." *Id*. at Abstract. Figure 2 is reproduced below.

FIG 3

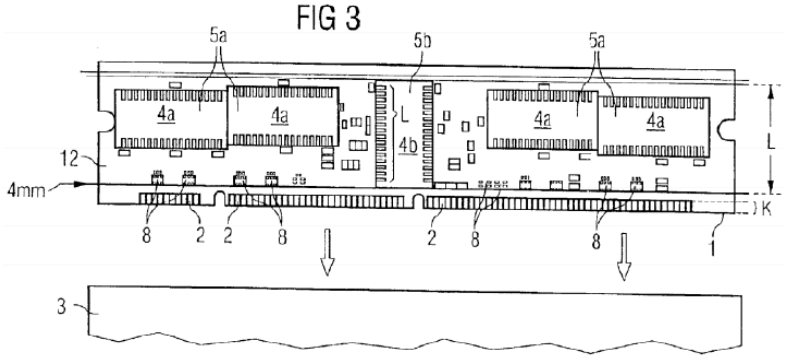

Figure 3 shows the rear side of a printed circuit board according to an embodiment of the '414 patent. *Id*. at 5:13–14. In this arrangement, housings 5a of semiconductor memories 4a are arranged horizontally on printed circuit board 1, and only housing 5b of error correction chip 4b is arranged vertically. *Id*. at 6:19–28. Housing 5b is "brought up

to [] contact strip 2 as close as possible" because "there is no need for any resistors 8 [between housing 5b and contact strip 2], as in the case of all of the other identically designed semiconductor memories 4*a* that are configured horizontally." *Id*. at 6:28–35. "As a result, the height of printed circuit board 1 can be reduced from a value of H_1 to a smaller value H_2" (*id*. at 6:41–42), as shown in Figure 2, which is reproduced below.

FIG 2

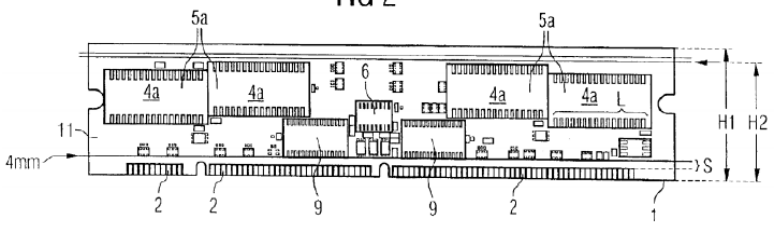

Figure 2 shows the front side of a printed circuit board according to an embodiment of the '414 patent. *Id*. at 5:11–12.

C. Illustrative Claim

Of the challenged claims, claim 1 is independent and claims 2–8 depend from claim 1. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. An electronic printed circuit board configuration, comprising:
>
> an electronic printed circuit board having a contact strip for insertion into another electronic unit; and
>
> a memory module having at least nine identically designed integrated semiconductor memories;

> each one of said semiconductor memories being encapsulated in a rectangular housing having a shorter dimension and a longer dimension;
>
> said housing of each one of said semiconductor memories being identically designed and being individually connected to said printed circuit board;
>
> one of said semiconductor memories being connected as an error correction chip;
>
> said longer dimension of said housing of said error correction chip being oriented perpendicular to said contact strip; and said longer dimension of said housing of each one of said semiconductor memories, other than said error correction chip, being oriented parallel with said contact strip.

Ex. 1001, 7:24–8:3.

D. Evidence Relied Upon

Petitioner relies upon the following prior art references:

> Simpson
>
> GB 2 289 573 A
>
> Nov. 22, 1995
>
> Ex. 1002
>
> PC SDRAM UNBUFFERED DIMM SPECIFICATION, REV. 1.0, 1997 (the "Intel Specification").
>
> Ex. 1003

Pet. 9. Petitioner also relies upon the Declaration of

Vivek Subramanian, Ph.D. ("Subramanian Decl.") (Ex. 1006).

E. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 9):

References	**Basis**	**Claims challenged**
Simpson	§ 103	1–8
Simpson and Intel Specification	§ 103	1–8
Intel	§ 103	1–8

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, a claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). We must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. Vi*vid Techs., Inc. v. Am. Sci.*

& Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner proposes a construction for "error correction chip." Pet. 7–8. Patent Owner does not propose explicit constructions of any particular terms, but several of its arguments turn on the meaning of "identically designed," "connected," and "error correction chip." *See, e.g.*, Prelim. Resp. 23–34. On this record, and for purposes of this Decision, we determine that only the terms "connected" and "error correction chip" requires express construction.

1. "connected" (claim 1)

Patent Owner argues "Simpson's alleged error correction chip is not 'connected' to the [printed circuit board] as claimed," because it is mounted in a socket rather than soldered directly to the printed circuit board. Prelim. Resp. 31. Petitioner argues that "a socket is a type of connection." Pet. 22 (citing Subramanian Decl. ¶ 59). We agree with Petitioner. The '414 patent does not explicitly define "connected" and Patent Owner identifies nothing in the Specification to support a construction of that term to exclude connections via a socket.

On this record, and for purposes of this decision, we agree with Petitioner that the broadest reasonable interpretation of "connected" encompasses being connected to the printed circuit board via a socket.

2. "error correction chip" (claim 1)

Petitioner argues that "error correction chip" should be construed to mean "a chip that is able to perform at least error checking on data stored in other semiconductor memories." Pet. 7–8. Patent

Owner argues that the term "error correction chip" excludes Simpson's parity memory device because a parity memory device "may provide 'error ***detection***,' [but] cannot perform 'error ***correction***.'" Prelim. Resp. 32–33. Patent Owner's argument is not persuasive. The '414 patent does not expressly define the term "error correction chip." The '414 patent describes the error correction chip as "check[ing] the correctness of the data," but not necessarily correcting errors:

> Data that is transported to the semiconductor memory modules 4*a* always contain check data. The error correction chip, namely memory module, 4*b* checks the correctness of the data before the data are passed on.

Ex. 1001, 7:1–4. More importantly, the '414 patent expressly discloses an example in which the "error correction" method is merely a check bit, i.e., a parity bit, that is added to the data to be communicated to the memory module:

> A wide variety of methods are known according to which the error correction chip, namely memory module, 4b can operate. An example that shall be mentioned here is the ECC method (error correcting code), in which *a check bit* is added to eight bits of data to be communicated.

Ex. 1001, 7:5–9 (emphasis added). This is consistent with Simpson's description of the parity bit, which "is assigned to every group of eight data bits of memory." Ex. 1002, 3:9–13. Because the '414 patent expressly contemplates "a check bit" as one of the

"ECC method[s]" that may be employed by the claimed "error correction chip," we are persuaded that the '414 patent uses the term "error correction" broadly enough to encompass parity.

On this record, and for purposes of this decision, we agree with Petitioner that the broadest reasonable interpretation of "error correction chip" is "a chip that is able to perform at least error checking on data stored in other semiconductor memories."

B. Claims 1–8: Obviousness over Simpson

Petitioner argues that the challenged claims are unpatentable under 35 U.S.C. § 103(a) as obvious over Simpson alone or in view of the Intel Specification. Pet. 10–43.[1] In light of the arguments and evidence of record, we are persuaded that Petitioner has established a reasonable likelihood that the claims 1 and 5–8 are unpatentable as obvious over Simpson.

1. Simpson (Ex. 1002)

Simpson describes a memory module with memory devices and with sockets on one or both faces of the module for coupling additional memory modules. Ex. 1002, [57]. Figures 1 and 3 of Simpson are reproduced below.

[1] Petitioner cites the Intel Specification only with respect to claims 3, 4, and 8. Pet. 33–34 (claim 3), 36–37 (claim 4), 42–43 (claim 8). Accordingly, we first analyze claims 1–8 for obviousness over Simpson. In the next section, we analyze claims 3, 4, and 8 for obviousness over Simpson and the Intel Specification.

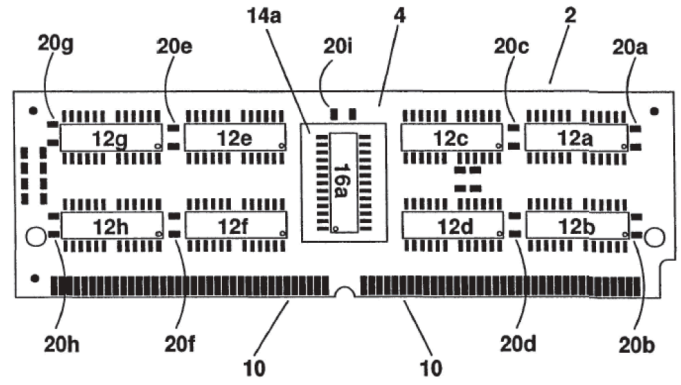

Fig 1

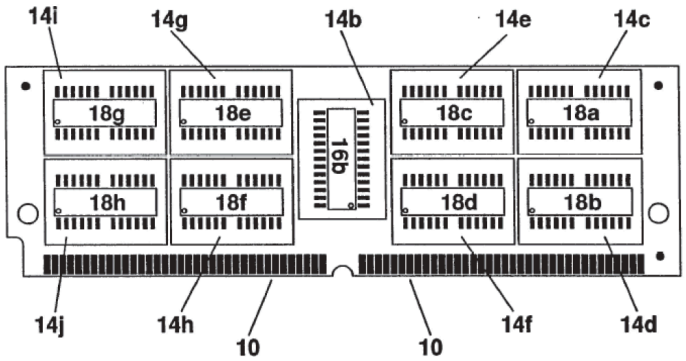

Fig 3

Figures 1 and 3 depict a front view and a rear view, respectively, of a memory module according to Simpson. *Id*. at 12:19–26. As shown in Figure 1, printed circuit board 2 includes memory devices 12A–H oriented horizontally to contact strip 10 and parity memory device 16A mounted in socket 14A oriented vertically to contact strip 10. *Id*. at 9:18–10:17.

2. Claim 1

With respect to claim 1, Petitioner relies upon Simpson's printed circuit board 2 with contact strip 10 as teaching "an electronic printed circuit board having a contact strip," relies upon memory devices 12A–H and 16A as teaching "nine identically

designed integrated semiconductor memories," relies upon Figure 1 as teaching that memory devices 12A–H and 16A are "encapsulated in a rectangular housing," each of which is "identically designed" and "individually connected to said printed circuit board." Pet. 16–23. Petitioner relies upon Simpson's memory device 16A as teaching "an error correction chip," and relies upon Figure 1 as teaching memory device 16A "being oriented perpendicular to said contact strip," and memory devices 12A–H "being oriented parallel with said contact strip." Pet. 23–27.

Patent Owner argues that (1) Simpson is not directed towards reducing the height of a printed circuit board (Prelim. Resp. 12–15); (2) Simpson does not teach nine "identically designed" semiconductor memories with "identically designed" housings (*id*. at 18, 24–31); (3) Simpson's alleged "error correction chip" is not "connected" to the printed circuit board (*id*. at 18, 31–32); and (4) Simpson's alleged "error correction chip" performs only error detection, not error correction (*id*. at 18, 32–33). We address each argument in turn.

a. Reducing the height

Patent Owner argues that Simpson is not directed towards reducing the height of a printed circuit board. Prelim. Resp. 12–15. Patent Owner's argument is unpersuasive because it is not commensurate with the claims, which do not recite reducing the height of a printed circuit board.

b. "identically designed"

Patent Owner argues that "Petitioner never even argues, let alone attempts to show, that the purported 'error correction chip' in Simpson is

'identically designed' in comparison with the memory chips." Prelim. Resp. 25. To the contrary, Petitioner argues that "[t]hose of ordinary skill in the art would understand that the memory device 16A is identical to each of memory devices 12A-12H." Pet. 19 (citing Subramanian Decl. ¶ 48; Ex. 1002, 12:10–14, 22-28).

Patent Owner also argues that Simpson "teaches that these error correction auxiliary devices are logic devices and, therefore, are not identically designed to its other memory modules." Prelim. Resp. 25–26 (citing Ex. 1002, 14:8–10, 10:8–9, 3:30–34, claim 9). Although Patent Owner recognizes that "it is possible to design a system . . . where the error correction chip is 'identically designed' to the other memory modules" by placing the logic element elsewhere on the system, Patent Owner argues that a person of ordinary skill in the art "would *not* assume that built-in error correction logic exists elsewhere in any system using Simpson's [printed circuit board]." *Id.* at 27. Patent Owner also argues that the housing of memory devices 12A–H and the housing of memory device 16A are not "identically designed" because the housing of memory device 16A includes two extra pins. *Id.* at 28–29. The '414 patent, however, concedes expressly that "the components illustrated [in Figures 2 and 3]"—including memory modules 4a (the recited "semiconductor memories") and 4b (the recited "error correction chip")—"and their functions *correspond to the prior art*." Ex. 1001, 6:57–60 (emphasis added). As a result, even assuming that Simpson does not teach explicitly that memory devices 12A–H and its memory device 16A are not "identically designed," we are nevertheless persuaded that Petitioner is

correct in asserting that it would have been obvious to one of ordinary skill in the art at the time that memory devices 12A–H and memory device 16A could be "identically designed."

c. "connected"

Patent Owner argues that Simpson's alleged "error correction chip"—i.e., memory device 16A—is not "connected" to the printed circuit board because it is in socket 14A. Prelim. Resp. 31–32. This argument is not persuasive because it is based on a construction of "connected" that we declined to adopt for the reasons discussed above. We are persuaded by Petitioner's contention that "[o]ne of ordinary skill in the art would understand that connection of a memory chip via a socket is a type of connection." Pet. 22 (citing Subramanian Decl. ¶ 60).

d. "error correction chip"

Patent Owner argues that Simpson's memory device 16A—i.e., a parity memory device—is not an "error correction chip" because it "may provide 'error ***detection***,' [but] cannot perform 'error ***correction***.'" Prelim. Resp. 32–33. This argument is not persuasive because it is based upon a construction of "error correction chip" that we declined to adopt for the reasons discussed above. We are persuaded that the '414 patent uses "error correction chip" to encompass parity devices and, therefore, are persuaded by Petitioner's contention that Simpson's memory device 16A, described as a parity memory device, teaches an "error correction chip."

At this stage in the proceeding, we are persuaded by Petitioner's explanations and supporting evidence regarding independent claim 1.

Based on the record before us, Petitioner has demonstrated a reasonable likelihood that it would prevail on its assertion that independent claim 1 would have been obvious over Simpson.

3. Dependent claims 5–8

We have reviewed Petitioner's explanations and supporting evidence regarding dependent claims 5–8 and find them persuasive. *See* Pet. 38–43. Patent Owner does not argue separately dependent claims 5–8. Based on the record before us, Petitioner has demonstrated a reasonable likelihood that it would prevail on its assertion that claims 5–8 would have been obvious over Simpson.

4. Dependent claims 2-4

Dependent claim 2 recites "said housing of said error correction chip extends a greater distance away from said contact strip than said housing of each one of said semiconductor memories, other than said error correction chip." Ex. 1001, 8:4–8. Petitioner, recognizing that Simpson's memory chips 12A, C, E, and G, extend a greater distance away from contact strip 10 than does the housing of memory device 16A, argues that "by omitting memory devices 12A, [C], E, and G and 18A, C, E, and G (as Simpson describes), the error correction chip (16A) extends a greater distance away from said contact strip than said housing of each one of said semiconductor memories" (Pet. 30), and includes the annotated figure reproduced below:

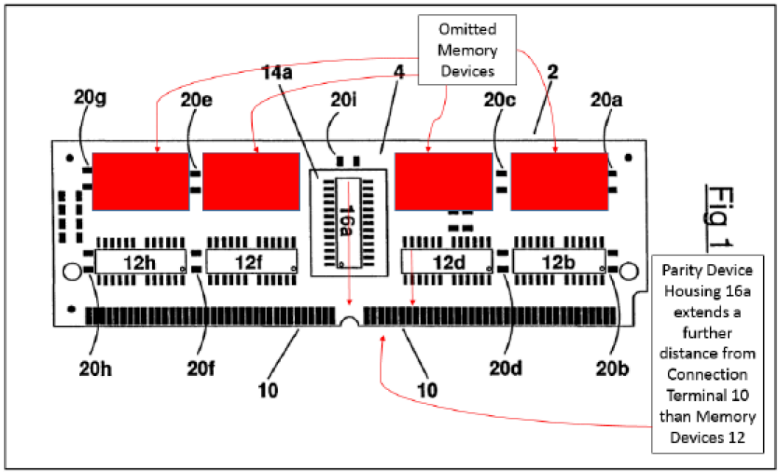

Fig. 1

According to Petitioner, the teaching of two rows in Simpson "is simply a matter of design choice" (Pet. 29) and "[o]ne of ordinary skill in the art would understand that the module design could choose to include or omit any of the various individual memory chips" (*id.* at 28). *See also id.* at 30 (arguing design choice).

Patent Owner argues that, although Petitioner "argues that a [person of ordinary skill in the art] would be *able* to make such a modification," Petitioner "does not propose a *single* reason why a [person of ordinary skill in the art] would be *motivated to make* this particular modification." Prelim. Resp. 35–36. We agree. It is not sufficient to demonstrate that each of a claim's limitations is known. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) ("a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art"). Petitioner must also explain how a person of ordinary skill in

the art would combine those embodiments and why such a person would be motivated to do so. *In re Chaganti*, 2014, WL 274514, *4 (Fed. Cir. 2014) ("It is not enough to say that . . . to do so would 'have been obvious to one of ordinary skill.' Such circular reasoning is not sufficient–more is needed to sustain an obviousness rejection."). Here, Petitioner has not explained sufficiently *why* a person of ordinary skill in the art would have modified Simpson to omit memory devices 12A, C, E, and G. Accordingly, on the record before us, we are not persuaded that Petitioner has provided an articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *See KSR*, 550 U.S. 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). As a result, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claim 2 would have been obvious over Simpson.

For claim 3, Petitioner relies upon the same proposed modification as in claim 2. *See, e.g.*, Pet 33 (explaining for claim 3 that "capacitors 20 . . . could be moved into the empty space provided by the omission of several memory devices or sockets as explained supra"). Thus, for the same reasons explained above with respect to claim 2, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claim 3 would have been obvious over Simpson.

Claim 4 recites, "said printed circuit board has a height of 1 to 1.2 inches perpendicular to said contact strip." Petitioner argues that a person of ordinary skill in the art would have had a reasonable

expectation of success in limiting Simpson to a height of 1 to 1.2 inches and would have been motivated to do so because, *inter alia*, "engineers have historically sought to reduce the size of electronic components." Pet. 35–36. Patent Owner argues that Petitioner "does not even explain how Simpson's two rows of sockets could fit on a [printed circuit board] with a height of 1.0-1.2 inches." Prelim. Resp. 39. According to Patent Owner, Simpson teaches "sockets arranged in two rows with dimensions that are significantly larger than the chip package itself . . . significantly increasing the height of the [printed circuit board." *Id.* at 41. We agree that Petitioner has not explained sufficiently how or why a person of ordinary skill in the art would have modified Simpson to achieve a height of "1 to 1.2 inches perpendicular to said contact strip." *Id.* at 39. As a result, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claim 4 would have been obvious over Simpson.

5. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1 and 5–8 are unpatentable as obvious over Simpson alone.

C. Claims 3, 4, and 8: Obviousness over Simpson and the Intel Specification

Petitioner argues that the challenged claims are unpatentable under 35 U.S.C. § 103(a) as obvious over Simpson in view of the Intel Specification. Pet. 10–43. Petitioner cites the Intel Specification, however, only with respect to claims 3, 4, and 8. Pet.

33–34, 36–37, 42. Accordingly, we analyze only claims 3, 4, and 8 for obviousness over the combination of Simpson and the Intel Specification. In light of the arguments and evidence of record, we are not persuaded that Petitioner has established a reasonable likelihood that the claims 3 and 4 are unpatentable as obvious over the combination of Simpson and the Intel Specification. Also, we decline to institute this ground as to claim 8.

1. Intel Specification (Ex. 1003)

The Intel Specification describes "the electrical and mechanical requirements for 168-pin, 3.3 volt, 64-bit and 72-bit wide, 4 clock, unbuffered Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs)." Ex. 1003, 7. "This specification largely follows the JEDEC defined 168-pin unbuffered SDRAM DIMM as of JEDEC committee meeting of December 1996." *Id*. The Intel Specification "give[s] the specific dimensions and tolerances for a 168-pin DIMM." *Id*. at 11.

2. Claims 3 and 4

As discussed above, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 3 and 4 would have been obvious over Simpson because it has not explained adequately how and/or why a person of ordinary skill in the art would have made the proposed modifications to Simpson. In this ground, Petitioner cites the Intel Specification for its teaching of a safety clearance of less than 2mm (Pet. 33–34 (for claim 3)) and for its teaching of a height in the range of 1 to 1.2 inches (Pet. 36–37 (for claim 4)). In both cases, however, Petitioner continues to

rely solely on its argument that the limitations would have been an "obvious design choice" without explaining persuasively how and/or why a person of ordinary skill in the art would have made the proposed modifications to Simpson in view of the teachings of the Intel Specification. As a result, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 3 and 4 would have been obvious over the combination of Simpson and the Intel Specification.

3. Claim 8

The Board's rules for AIA *inter partes* proceedings, including those pertaining to institution, are "construed to secure the just, speedy, and inexpensive resolution of every proceeding." 37 C.F.R. § 42.1(b); *accord* 35 U.S.C. §§ 316(b) (regulations for AIA *inter partes* proceedings take into account "the efficient administration of the Office" and "the ability of the Office to timely complete [instituted] proceedings"). Because we institute an *inter partes* review of claim 8 based on the ground discussed above, we exercise our discretion not to institute a review based on this ground for reasons of administrative expediency to ensure timely completion of the instituted proceeding. *See* 37 C.F.R. § 42.108(a) ("the Board may authorize the review to proceed . . . on all or some of the grounds of unpatentability asserted for each claim"); 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1368 (Fed. Cir. 2016) ("[U]nder [37 C.F.R. §

42.108(a)], it is clear that the Board may choose to institute some grounds and not institute others as part of its comprehensive institution decision.").

D. Claims 1–8: Obviousness over the Intel Specification

Petitioner argues that the challenged claims are unpatentable under 35 U.S.C. § 103 as obvious over the Intel Specification. Pet. 9.

Claim 1 recites "said longer dimension of said housing of each one of said semiconductor memories, other than said error correction chip, being oriented parallel with said contact strip." Petitioner relies on Intel's teaching of an embodiment in which memory devices are oriented parallel to a contract strip. Pet. 51 (citing Ex. 1003, 34). Petitioner contends that

> One of ordinary skill would recognize that there is nothing novel about the orientation of semiconductor memories and that it would be obvious to arrange memories on a printed circuit board as necessary in any orientation within the specification limitations set forth by the Intel Specification. Ex. 1006, Subramanian Decl. at ¶137; *see also* MPEP 2143(A) (Combining prior art teaching (vertical vs horizontal orientations) according to known methods to produce predictable results—it would be predictable that a horizontal orientation would yield a shorter height for a PCB.); MPEP 2143(E) ("obvious to try" choosing from a finite (horizontal or vertical) number of predictable solutions.).

Moreover, the Intel Specification recognizes

> that a printed circuit board could have "components mounted on one or both sides of the PCB." Ex. 1003, Intel Specification at 34. With that said, one of ordinary skill in the art would also understand that there would be no physical constraints to moving four of the memory components from the Intel memory module to the back side with a horizontal orientation. Ex. 1006, Subramanian Decl. at ¶137.

Id. at 51–52.

Patent Owner argues that "[t]he Petition further fails to articulate even a single reason why a [person of ordinary skill in the art] would modify the Intel Specification in the manner proposed to arrive at the claimed invention" and, instead, "simply makes conclusory assertions that a POSITA could make the proposed modifications and would have a reasonable expectation of success in doing so." Prelim. Resp. 50, 54.

We agree. The embodiment relied upon by Petitioner for this limitation is different from the embodiment relied upon by Petitioner for earlier limitations of claim 1. Petitioner does not explain sufficiently *why* a person of ordinary skill in the art would have combined the two embodiments, or otherwise would have modified the first embodiment such that each one of the semiconductor memories, other than the error correction chip, is oriented parallel with the contact strip. As a result we are not persuaded that Petitioner has provided an articulated reasoning with some rational underpinning to support the legal conclusion of

obviousness. *See KSR*, 550 U.S. 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

On this record, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claim 1, or claims 2–8 which depend therefrom, would have been obvious over the Intel Specification.

E. Claims 1–8: Obviousness over the Intel Specification and Simpson

Petitioner asserts that the challenged claims are unpatentable under 35 U.S.C. § 103 as obvious over the Intel Specification and Simpson. Pet. 64. This alleged ground, however, consists solely of the following sentence: "For the same reasons outlined in Subsection X, Subparts A and B, claim 1-8 of the '414 patent are rendered obvious by the Intel Specification in view of Simpson as well. Ex. 1006, Subramanian Decl. at ¶162."

Because we institute an *inter partes* review of claims 1 and 5–8 based on the ground discussed above, we exercise our discretion not to institute a review based on this ground for reasons of administrative expediency to ensure timely completion of the instituted proceeding. *See* 37 C.F.R. § 42.108(a) ("the Board may authorize the review to proceed . . . on all or some of the grounds of unpatentability asserted for each claim"); 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1368 (Fed. Cir. 2016) ("[U]nder [37 C.F.R. § 42.108(a)], it is clear that the Board may choose to

institute some grounds and not institute others as part of its comprehensive institution decision.").

With respect to claims 3 and 4, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–8 would have been obvious over the Intel Specification for the reasons discussed above. As also discussed above, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 3 and 4 would have been obvious over the combination of Simpson and the Intel Specification. In this ground, Petitioner provides no additional explanation or evidence regarding how and why a person of ordinary skill in the art would have combined Simpson and the Intel Specification to arrive at claims 3 and 4. As a result, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 3 and 4 would have been obvious over the Intel Specification and Simpson.

III. CONCLUSION

For the foregoing reasons, we are persuaded that Petitioner has demonstrated that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1 and 5–8 of the '414 patent. At this stage of the proceeding, we have not made a final determination with respect to the patentability of these challenged claims or to the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted as to claims 1 and 5–8 under 35 U.S.C. § 103(a) as obvious over Simpson;

FURTHER ORDERED that no other grounds are authorized for this *inter partes* review other than those specifically identified above; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(d) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial commences on the entry date of this Decision.

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APPENDIX I

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE
PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,
v.
POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01622
Patent 6,850,414 B2

Before SALLY C. MEDLEY, JEAN R. HOMERE, and KEN B. BARRETT, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background and Summary

Kingston Technology Company, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–8 of U.S. Patent No. 6,850,414 B2 ("the '414 patent," Ex. 1001). Paper 2 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") [1] filed a Preliminary Response to the Petition. Paper 6 ("Prelim. Resp."). The Board instituted *inter partes* review (Paper 7, "Inst. Dec.") of claims 1 and 5–8 on the ground of obviousness under 35 U.S.C. § 103(a) over Simpson[2]. The Board did not institute a review as to dependent claim 4. Petitioner filed a Request for Rehearing of The Board's Institution Decision on Claim 4 (Paper 11), which was denied (Paper 16).

Patent Owner filed a Motion to Amend seeking to cancel the instituted challenged claims and proposing to substitute a newly-presented claim 9 for dependent claim 8. Paper 18 ("MTA"). Patent Owner did not file a Response to the Petition. Subsequently, Petitioner filed an Opposition to Patent Owner's Motion to Amend (Paper 20, "MTA Opp."), and Patent Owner filed a Reply to Petitioner's Opposition to Motion to Amend (Paper 23, "MTA Reply").

On October 4, 2017, the Federal Circuit issued an *en banc* decision in *Aqua Products, Inc. v. Matal*, 872 F.3d 1290 (Fed. Cir. 2017) addressing the burden of proof that the Board applies when

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[1] Patent Owner identifies Polaris Innovations Ltd., Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 4, 1; Paper 19, 1.

[2] UK Patent Application GB 2 289 573 A, published Nov. 22, 1995 (Ex. 1002).

considering the patentability of substitute claims presented in a motion to amend filed under 35 U.S.C. § 316(d).

Pursuant to our authorization (Paper 25), Petitioner filed a Surreply to Patent Owner's Motion to Amend (Paper 28, "MTA Surreply"). Thereafter and pursuant to our authorization (Paper 29), Patent Owner filed a Brief Addressing Impact of *Aqua Products v. Matal* (Paper 30).

An oral hearing was held on November 14, 2017, and a transcript of the hearing is included in the record. Paper 34 ("Tr.").

B. Related Proceedings

According to the parties, the '414 patent is involved in *Polaris Innovations Ltd. v. Kingston Tech. Co., Inc.*, Case No. 8:16-cv-300 (C.D. Cal.). Pet. 1; Paper 4, 1.

Petitioner filed a petition seeking *inter partes* review of claim 4 of the '414 patent in Patent Trial and Appeal Board Case IPR2017-00974 (Paper 2). In that case, the Board exercised its discretion under 35 U.S.C. §§ 314(a) and 325(d) to not institute an *inter partes* review. IPR2017-00974, Paper 8. Petitioner's request for reconsideration of that decision was denied. IPR2017-00974, Papers 9, 11.

C. The '414 Patent

The '414 patent, titled "Electronic Printed Circuit Board Having a Plurality of Identically Designed, Housing-Encapsulated Semiconductor Memories," issued February 1, 2005, from U.S. Patent Application No. 10/187,763. Ex. 1001 at [54], [45], [21].

The ’414 patent generally relates to an electronic printed circuit board having a memory module comprised of identically designed semiconductor memories configured on the printed circuit board. *Id.* at Abstract. “Printed circuit boards of this type are inserted into motherboards of personal computers or network computers and serve as the main memory.” *Id.* at 1:21–23. Figures 1A and 1B are reproduced below.

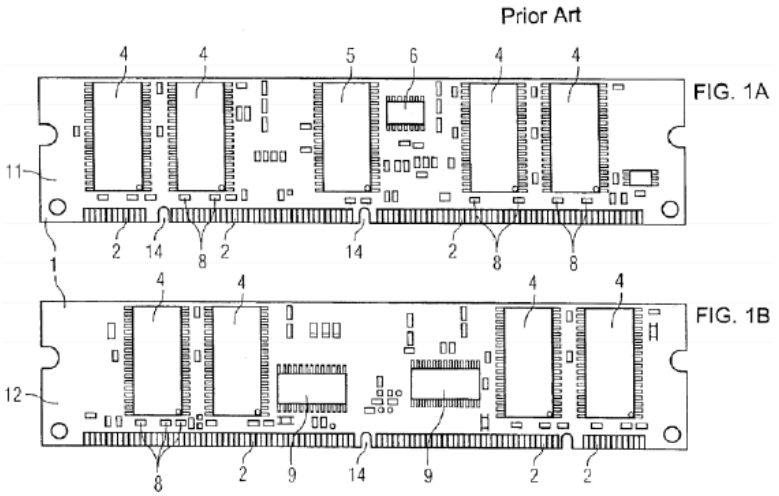

Figure 1A shows the front side of a conventional printed circuit board and Figure 1B shows the rear side of a conventional printed circuit board. *Id.* at 5:6–10. According to the ’414 patent, in a conventional arrangement, semiconductor memories 4 are arranged on the front and rear sides of the printed circuit board in the same orientation as error correction chip 5. *Id.* at 1:62–67. “In the case of this conventional arrangement . . . there is no more leeway for a further reduction of the circuit board height (the height of the printed circuit board perpendicular to the contact strip).” *Id.* at 2:37–41.

In network computers, however, "the printed circuit boards are inserted into compartment-type elements having a small height, for which reason the printed circuit boards themselves should also have only a small height." *Id*. at 1:23–27.

To address this problem, the '414 patent discloses an electronic printed circuit board in which the error correction chip remains oriented perpendicular to the contact strip but the other semiconductor memories are oriented parallel to the contact strip, such that it is "possible to reduce the height of the printed circuit board while enabling the rectangular housing to keep the same physical form." *Id*. at Abstract. Figure 3 is reproduced below.

FIG 3

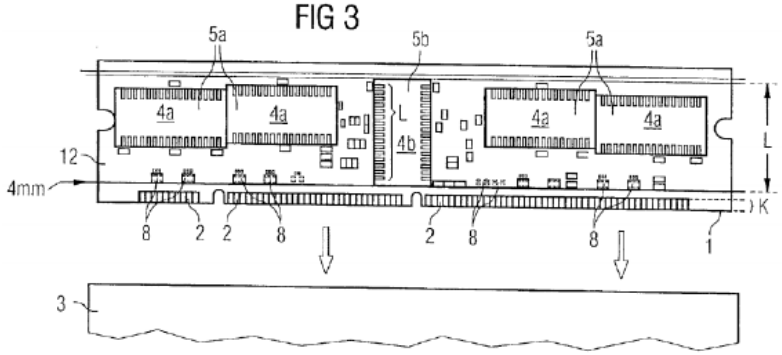

Figure 3 shows the rear side of a printed circuit board according to an embodiment of the '414 patent. *Id*. at 5:13–14. In this arrangement, housings 5a of semiconductor memories 4a are arranged horizontally on printed circuit board 1, and only housing 5b of error correction chip 4b is arranged vertically. *Id*. at 6:19–28. Housing 5b is "brought up to [] contact strip 2 as close as possible" because "there is no need for any resistors 8 [between housing 5b and contact strip 2], as in the case of all

of the other identically designed semiconductor memories 4a that are configured horizontally." *Id*. at 6:28–35. "As a result, the height of printed circuit board 1 can be reduced from a value of H1 to a smaller value H2" (*id*. at 6:41–42), as shown in Figure 2, which is reproduced below.

FIG 2

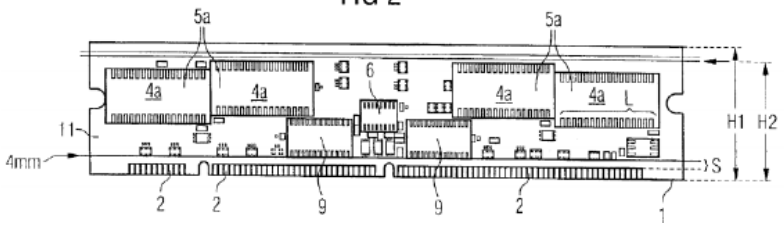

Figure 2 shows the front side of a printed circuit board according to an embodiment of the '414 patent. Id. at 5:11–12.

D. Illustrative Claim

Claim 1 of the '414 patent is an independent claim. Claims 2–8 all depend directly from Claim 1. Claim 1, reproduced below, is illustrative:

> 1. An electronic printed circuit board configuration, comprising:
>
> an electronic printed circuit board having a contact strip for insertion into another electronic unit; and
>
> a memory module having at least nine identically designed integrated semiconductor memories;
>
> each one of said semiconductor memories being encapsulated in a rectangular housing having a shorter dimension and a longer dimension;

> said housing of each one of said semiconductor memories being identically designed and being individually connected to said printed circuit board;
>
> one of said semiconductor memories being connected as an error correction chip;
>
> said longer dimension of said housing of said error correction chip being oriented perpendicular to said contact strip; and
>
> said longer dimension of said housing of each one of said semiconductor memories, other than said error correction chip, being oriented parallel with said contact strip.

Ex. 1001, 7:24–8:3.

II. ANALYSIS OF THE INSTITUTED CHALLENGE

A. Principles of Law

Petitioner bears the burden of proving unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish the facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398,

406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. The Level of Ordinary Skill in the Art

Petitioner's expert, Dr. Vivek Subramanian, opines that "a person of ordinary skill in the art as of the time of the '414 Patent would have a Bachelor's degree in Electrical Engineering and at least 2 years' experience working in the field of semiconductor memory design." Ex. 1006 ¶ 17; see Pet. 5–6 (citing the same). This definition is consistent with the level of ordinary skill reflected in the prior art references of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect an appropriate level of skill in the art). Patent Owner does not dispute Petitioner's definition. We adopt Dr. Subramanian's definition of the person of ordinary skill in the art.

C. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire patent disclosure. *In re*

Translogic Tech., Inc., 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. Individually Connected

Claim 1 recites "said housing of each one of said semiconductor memories . . . being *individually connected* to said printed circuit board" and "one of said semiconductor memories being *connected* as an error correction chip." Ex. 1001, 7:33–37 (emphasis added).

In the Institution Decision, we addressed the construction of the claim term "connected" due to the parties' arguments concerning the Simpson reference. Inst. Dec. 7–8. Patent Owner argued in its Preliminary Response that Simpson does not teach "'connecting' an error correction chip to the PCB [printed circuit board] as claimed," because the Simpson chip identified by Petitioner as an error correction chip is mounted in a socket rather than soldered directly to the printed circuit board. Prelim. Resp. 31. Petitioner argued that "a socket is a type of connection." Pet. 22–23 (citing Ex. 1006 ¶ 60). We agreed with Petitioner, noting that the '414 patent does not explicitly define "connected" and Patent Owner identified nothing in the Specification to support a construction of that term to exclude connections via a socket. Inst. Dec. 8. Accordingly, we determined, for purposes of the Institution Decision, "the broadest reasonable interpretation of 'connected' encompasses being connected to the printed circuit board via a socket." *Id.*

Patent Owner, in its reply to Petitioner's opposition to the Motion to Amend, impliedly argues that the modifier "individually" means the memory

housings must be *directly* connected to the printed circuit board. MTA Reply 10. Specifically, Patent Owner argues that being connected through "an intermediary with receptacles" is not "directly connected" and thus Simpson lacks the recited "individually connected" semiconductor memory housings in that "Simpson's alleged memory chips are connected to sockets, that are in turn connected to its printed circuit board." *Id*. at 10–11 (citations omitted). Patent Owner asserts that its proposed construction of "individually" as meaning "directly" is supported by a purported admission of Petitioner's expert, Dr. Subramanian, during cross examination. *Id*. (citing Ex. 2012 (Subramanian Dep. Tr.), 234:6–237:22; Ex. 2013 (deposition exhibit)). We have reviewed the cited pages of the deposition transcript and agree with Petitioner that that portion of the deposition involves a "confusing hypothetical arrangement" (MTA Surreply 1–2). Patent Owner does not explain adequately or persuasively how this ambiguous extrinsic evidence supports its argument that the claim phrase "individually connected" should be construed as limited to direct connections.

Having considered the parties' arguments and the complete record, we again determine that the broadest reasonable interpretation of "connected" encompasses being connected to the printed circuit board via a socket, and further determine that the claim term "individually" does not require the subject components to be directly connected.

2. Error Correction Chip

In the Institution Decision, we indicated that we were persuaded that the '414 patent uses, in

independent claim 1, the term "error correction" broadly enough to encompass parity, and we preliminarily construed "error correction chip" as "a chip that is able to perform at least error checking on data stored in other semiconductor memories." Inst. Dec. 8–9 (quoting Ex. 1001, 7:1–9). Although Patent Owner did not propose in the Preliminary Response an explicit construction for the term, we determined that a preliminary construction in the Institution Decision was necessary due to Patent Owner's arguments concerning claim 1. *Id*. at 7. After issuance of the Institution Decision, Patent Owner did not address further the meaning of the term, and it appears that it no longer is in dispute. We adopt that earlier construction in this Final Decision.

D. The Instituted Challenge: The Alleged Obviousness of Claims 1 and 5–8 over Simpson

As mentioned above, we instituted an *inter partes* review of Petitioner's challenge to claims 1 and 5–8 as being obvious over Simpson. Inst. Dec. 23; see Pet. 10–27. In the Petition, Petitioner relied upon the Declaration of Vivek Subramanian, Ph.D. (Ex. 1006). *See, e.g.*, Pet. 9–10. Patent Owner did not file a response to the petition after the decision on institution, but did file a Motion to Amend. In that motion, which we deny for the reasons discussed below, Patent Owner requests the cancellation of the instituted claims 1 and 5–8 and proposes the entry of a substitute claim. MTA 1. By not filing a response to the Petition, and requesting cancellation of claims 1 and 5–8 not based on any apparent contingency, Patent Owner has waived any argument that the challenged claims for which we instituted review—

claims 1 and 5–8 of the '414 patent—would not have been obvious over Simpson. *See, e.g.*, Paper 8, 3 (Scheduling Order stating: "The patent owner is cautioned that any arguments for patentability not raised and fully briefed in the response will be deemed waived."). Nonetheless, we review anew Petitioner's arguments and the evidence concerning the obviousness challenge to claims 1 and 5–8 and we consider Patent Owner's arguments (*see* MTA Reply 10–11), made in the context of the Motion to Amend, concerning limitations of at least claim 1 that necessarily are incorporated in proposed substitute claim 9 by virtue of its dependency from independent claim 1.

1. Simpson (Ex. 1002)

Simpson describes a memory module with memory devices and with sockets on one or both faces of the module for coupling additional memory modules. Ex. 1002, [57]. Figures 1 and 3 of Simpson are reproduced below.

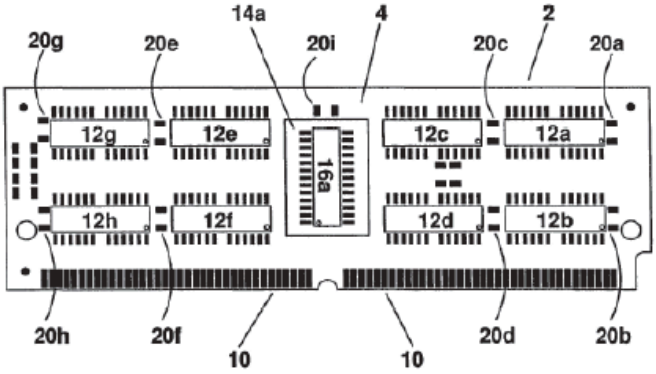

Fig 1

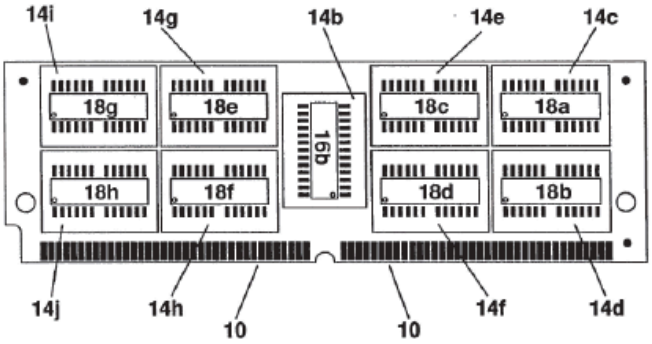

Fig 3

Figures 1 and 3 depict a front view and a rear view, respectively, of a memory module according to Simpson. *Id*. at 12:19–26. As shown in Figure 1 (in which lowercase letters are used in element numbers), a printed circuit board includes memory devices 12A–12H oriented horizontally to connector terminal strip 10 and parity memory device 16A mounted in socket 14A oriented vertically to connector terminal strip 10. Id. at 9:18–10:17. "The memory devices 12A–12H are electrically and mechanically connected to the substrate 4." *Id*. at 10:1–2. "In addition to the memory devices 12A–12H, the sockets 14A–14J to take additional devices are also attached to the substrate 4." *Id*. at 10:5–7.

2. Independent Claim 1

With respect to claim 1, Petitioner asserts, and we agree, that Simpson's printed circuit board with connector terminal strip 10 teaches the claim's recited "electronic printed circuit board having a contact strip." *See* Pet. 16–18; Ex. 1006 ¶¶ 42–46.

Petitioner relies upon Simpson's memory devices 12A–12H and 16A as teaching the recited "at least nine identically designed integrated semiconductor memories," and relies upon Figure 1 as teaching that memory devices 12A–12H and 16A are "encapsulated in a rectangular housing," each of which is "identically designed" and "individually connected to said printed circuit board." Pet. 18–22; Ex. 1006 ¶¶ 47–61. In this regard, Petitioner, relying on the testimony of Dr. Subramanian, persuasively asserts that "[t]hose of ordinary skill in the art would understand that the memory device 16A is identical to each of memory devices 12A-12H," and, alternatively, that it would have been obvious to one of ordinary skill in the art to use identically designed memory and error correction chips. Pet. 19 (citing Ex. 1006 ¶ 48; Ex. 1002, 10:22-28, 12:10–14); *id.* at 25–26 (citing Ex. 1006 ¶¶ 63–64). As discussed above, we have declined to adopt a construction of "individually connected" that would exclude an indirect connection. Petitioner notes that "Simpson further discloses that the 'memory devices 12A-12H are electrically and mechanically connected to the substrate 4.'" Pet. 22 (quoting Ex. 1002, 10:1-5). Regarding Simpson's disclosure of the use of sockets on the circuit board, we also are persuaded by Petitioner's contention that "[o]ne of ordinary skill in the art would understand that connection of a memory chip via a socket is a type of connection."

Pet. 22 (citing Ex. 1006 ¶ 60).

Petitioner asserts, and we agree, that Simpson's parity memory device 16A is "an error correction chip," and that Figure 1 teaches memory device 16A "being oriented perpendicular to said contact strip." Pet. 23–27; Ex. 1006 ¶¶ 62–66.

Lastly, Petitioner notes that Simpson's Figure 1 depicts memory devices 12A–12H "being oriented parallel with said contact strip." Pet. 27; Ex. 1006 ¶¶ 67–69.

We are persuaded by Petitioner's showing, and adopt it as our own, that Simpson renders obvious independent claim 1.

3. Dependent Claims 5–8

Patent Owner, in its Preliminary Response to the Petition, did not present separate arguments for dependent claims 5–8 and Patent Owner did not submit a response to the Petition after institution. We have reviewed Petitioner's explanations and supporting evidence regarding dependent claims 5–8, *see* Pet. 38–43, and we determine that Petitioner has shown by a preponderance of the evidence that dependent claims 5–8 are unpatentable under 35 U.S.C. § 103 over Simpson.

III. MOTION TO AMEND

A. Proposed Substitute Claim

Patent Owner filed a Motion to Amend and moves to cancel all the instituted challenged claims—claims 1 and 5 through 8—and to substitute new claim 9 for challenged claim 8. MTA 1, 2, Appendix. Proposed substitute claim 9 adds to claim

8 (which depends directly from independent claim 1) the printed circuit board height limitation of dependent claim 4 (which also depends directly from independent claim 1). Proposed substitute claim 9 is reproduced below with underlining indicating text added to dependent claim 8.

> 9. The printed circuit board according to claim 1, wherein:
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> said printed circuit board has a width of 5.25 inches and has a height of 1 to 1.2 inches perpendicular to said contact strip.

MTA, Appendix. As a dependent claim, proposed substitute claim 9 necessarily includes all the limitations of independent claim 1 from which it depends.

We note that this is not simply a case where Patent Owner seeks to rewrite dependent claim 4 in independent form. Because dependent claim 4 and dependent claim 8—which together now form proposed substitute claim 9—both depend directly from independent claim 1, the Motion to Amend is the first time that the width and height limitations have appeared in the same claim. *See* Tr. 86:3–20.

B. Motions to Amend in view of Aqua Products

On October 4, 2017, the Federal Circuit issued an *en banc* decision in *Aqua Products, Inc. v. Matal*, 872 F.3d 1290 (Fed. Cir. 2017). In light of the *Aqua Products* decision, the Board will not place the burden of persuasion on a patent owner with respect to the patentability of substitute claims presented in a motion to amend. *Aqua Products*, 872 F.3d at 1327; *see also* "Guidance on Motions to Amend in view of

Aqua Products" (Nov. 21, 2017) (https://www.uspto.gov/sites/default/files/documents/guidance_on_motions_to_amend_11_2017.pdf) ("Guidance"). A motion to amend still must meet the statutory requirements of 35 U.S.C. § 316(d) and the procedural requirements of 37 C.F.R. § 42.121. *See* Guidance.

Because, for the reasons set forth below, we determine that the proposed substitute claim is not patentable, we do not need to determine whether the Motion to Amend meets the requirements of 35 U.S.C. § 316(d) and 37 C.F.R. § 42.121.

C. The Alleged Untimeliness of Petitioner's Arguments in Opposition to the Motion to Amend

Patent Owner argues that Petitioner's arguments in opposition to the Motion to Amend and proposed substitute claim 9 are untimely attacks on dependent claim 4, and urges that we proceed immediately to a determination that the proposed substitute claim 9 is patentable without further input from Petitioner after the decision declining to institute a review of dependent claim 4. *See* MTA Reply 1, 5, 9. In effect, Patent Owner contends that Petitioner should have made its case for unpatentability of the proposed amended claim 9 in the Petition and that Petitioner now should be foreclosed from opposing the Motion to Amend.

Patent Owner's position apparently is premised on several misconceptions based on the denial of institution as to Petitioner's challenges to claim 4. For example, Patent Owner implies that we conclusively ruled on the merits of the patentability of claim 4 at the institution stage in this case and

that we found that the height limitation of claim 4 was not disclosed in the prior art. *See* MTA Reply 1 ("the Board has already rejected [Petitioner's] positions on the merits at least three times"); *id*. at 3 (emphasis omitted, "Claim 9 simply adds to the limitations of instituted Claim 8 the limitation of Claim 4—the exact same limitation that the Board has found, three times, not disclosed by Petitioner's references and arguments."); *id*. at 3 ("Patent Owner's Motion adds a substitute claim, Claim 9, that has a limitation the Board has already repeatedly found was not in the references raised by Petitioner. Patent Owner is entitled to rely on those prior rulings for purposes of its Motion to Amend."); MTA 3–4 ("the limitation that already appears in claim 4 has already been found to not have been shown by Petitioner in this case to be disclosed or suggested by the prior art.").

The decision on institution was made pursuant to 35 U.S.C. § 314, while our final written decision—including the consideration of the Motion to Amend—is made pursuant to a different statute, 35 U.S.C. § 318. Here, our analyses made in arriving at these two types of decisions are not the same. In our institution decision and as detailed below, we evaluated Petitioner's articulation of a case of obviousness (*see, e.g.*, Inst. Dec. 16–17), whereas we now must render a final written decision on the patentability of a proposed substitute claim not previously considered based on the entirety of the record, *see* 35 U.S.C. § 318(a) ("If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the

patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d)."); *see also Aqua Prods.*, 872 F.3d at 1296 ("The matter is remanded for the Board to issue a final decision under § 318(a) assessing the patentability of the proposed substitute claims without placing the burden of persuasion on the patent owner.").

Contrary to Patent Owner's implied arguments, we have neither determined affirmatively that dependent claim 4 is patentable nor found the height limitation missing from the prior art. Petitioner challenged, in the Petition, claims 1–8 of the '414 patent. As to dependent claim 4 (reciting the height limitation), we did not institute on the ground of obviousness over Simpson, stating "Petitioner has not explained sufficiently how or why a person of ordinary skill in the art would have modified Simpson to achieve a height of '1 to 1.2 inches perpendicular to said contact strip.'" Inst. Dec. 17 (quoting Ex. 1001, 8:19–20 ('414 patent, claim 4)). Similarly, we did not institute a review on the ground of Simpson in combination with the Intel Specification[3] because "Petitioner continues to rely solely on its argument that the limitations would have been an 'obvious design choice' without explaining persuasively how and/or why a person of ordinary skill in the art would have made the proposed modifications to Simpson in view of the teachings of the Intel Specification." *Id.* at 18; *see also id.* at 20–21, 22 (declining to institute as to other grounds based on inadequate reasoning). We

[3]PC SDRAM UNBUFFERED DIMM SPECIFICATION, Rev. 1.0, Feb. 1998 (the "Intel Specification") (Ex. 1003).

denied Petitioner's request for reconsideration, in pertinent part, because Petitioner had not addressed whether one of ordinary skill would have been able to fit two rows of chips on a circuit board having a height of only 1 to 1.2 inches. Paper 16, 6. Petitioner filed another petition challenging claim 4, and that second petition was the subject of a discretionary denial in light of the first petition. IPR2017-00974, Papers 2, 8. Petitioner's request for reconsideration of that decision was denied. IPR2017-00974, Papers 9, 11. In denying that request for reconsideration, we confirmed "[i]n neither decision [denying institution as to claim 4] did the Board determine affirmatively that claim 4 is patentable over the prior art asserted in the respective petitions." IPR2017-00974, Paper 9, 5. Accordingly, Patent Owner's reliance on those prior decisions is misplaced.

Patent Owner also argues that its desired outcome in this case is required by an unrelated Board decision, *Amerigen Pharms. Ltd. v. Shire LLC*, Case IPR2015-02009, Paper 38 (PTAB Mar. 31, 2017) (non-precedential) (Ex. 2011). MTA Reply 1, 6–8. In the *Amerigen* case, the panel granted a motion to amend after considering and finding unpersuasive the petitioner's arguments in opposition to the motion. *Amerigen*, slip op. 5–6. We fail to see how that fact-specific ruling supports Patent Owner's arguments that we should not consider Petitioner's arguments in this case. Additionally, Patent Owner acknowledges that a key consideration in the *Amerigen* panel's decision was the fact that the substitute claim "included only limitations of non-instituted or non-challenged claims." MTA Reply 7 (citing Ex. 2011, 4–5); *see Amerigen*, slip op. 5 ("the

practical effect of [the proposed substitution] would be to leave no instituted claim remaining in the trial."). In *Amerigen*, the panel stated that, "[e]ffectively, no claim [was] being amended, and claims [were] only being cancelled . . . ." *Amerigen*, slip op. at 6 (quoting the patent owner's argument; internal quotations omitted); *id.* at 6 ("With the cancellation of claims 18–25, and the entry of substitute claim 26, there would be no claim remaining subject to *inter partes* review in this proceeding."). That fact pattern is not present in the case before us. *Amerigen* does not, as Patent Owner implies, establish a procedural rule that precludes a petitioner from opposing a motion to amend.

Lastly, we note that—after the denials of institution as to claim 4 and at which point it no longer was involved in this inter partes review—Patent Owner did not remain silent as to that claim. Notwithstanding that Patent Owner's Motion to Amend reflects a willingness to cancel the instituted claims—a group which does not include claim 4—Patent Owner did not simply request to cancel the instituted claims and seek adverse judgment, which, if granted, would have ended this inter partes review and would have left claim 4 unaddressed ever again in this proceeding. Cf. Inst. Dec. 23; Tr. 88:7–8 (Patent Owner asserting: "Everyone agrees that had we not filed a motion to amend, you couldn't revisit the claim 4 decision in this case."). Rather, Patent Owner made a strategic decision to propose a substitute amended claim that includes the limitation of challenged and instituted dependent claim 8 along with the limitation of non-instituted dependent claim 4. Petitioner argues that Patent

Owner added the limitation of claim 4 back into the case in the form of proposed claim 9 in order for estoppel to attach to it, and thereby "materially harm[] the petitioners in District Court," and maintains that it would be a due process violation to attach estoppel based on a decision at the institution stage.[4] Tr. 74, 102; see also id. at 73– 74 (Petitioner drawing a distinction between an institution decision under 35 U.S.C. § 314 and a final written decision under § 318). Regardless as to the reasons underlying Patent Owner's actions, it is because of those actions that the height limitation of claim 4 is again involved in this proceeding.

After consideration of the parties' arguments and because Patent Owner has not directed our attention to any statute, rule,[5] or legal precedent that supports its position, we decline to foreclose an opposition to the Motion to Amend from Petitioner.

D. Patentability

As discussed above, Patent Owner does not have the burden of persuasion with respect to the patentability of the substitute claim presented in its Motion to Amend. *See Aqua Products*, 872 F.3d at 1327; *see also* Guidance. We determine whether the

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[4] *See Shaw Indus. Grp. Inc. v. Automated Creel Sys., Inc.*, 817 F.3d 1293, 1300 (Fed. Cir. 2016) (discussing estoppel and distinguishing between the pre-institution phase and the *inter partes* review, which "does not begin until it is instituted."). We express no opinion as to whether and to what extent estoppel would or would not apply in the hypothetical situation presented here.

[5] 37 C.F.R. § 42.20(d), under the heading "Petition and Motion Practice," states that "[t]he Board may order briefing on any issue involved in the trial." We have issued orders permitting briefing on the Motion to Amend. *See* Paper 8, 25, 29.

substitute claim is unpatentable by a preponderance of the evidence based on the entirety of the record, including any opposition made by the petitioner. *See Aqua Products*, 872 F.3d at 1325–26; *see also* Guidance. For the reasons explained below, considering the entirety of the record before us, we determine that the preponderance of the evidence shows that the proposed substitute claim is not patentable over the prior art of record. Specifically, we determine that proposed substitute claim 9 is unpatentable at least under 35 USC § 103(a) as obvious over Simpson (discussed above) and the Intel Specification.

1. The Intel Specification

The Intel Specification describes "the electrical and mechanical requirements for 168-pin, 3.3 volt, 64-bit and 72-bit wide, 4 clock, unbuffered Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs)." Ex. 1003, 7. "This specification largely follows the JEDEC[6] defined 168-pin unbuffered SDRAM DIMM as of JEDEC committee meeting of December 1996." *Id*. The Intel Specification "give[s] the specific dimensions and tolerances for a 168-pin DIMM." *Id*. at 11. The Intel Specification specifies that the overall length[7] of the

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[6] According to Petitioner: "JEDEC stands for the 'Joint Electron Device Engineering Council.' JEDEC is a recognized standard setting body within the industry. Specifically, the JEDEC memory standards are the specifications for semiconductor memory circuits and similar storage devices promulgated by JEDEC." Pet. 6 n.1.

[7] The printed circuit board "width" in the claims of the '414 patent corresponds to the "length" of the board in the Intel Specification. *See* Ex. 1001, 4:12–13 (The '414 patent explaining that "the length of the edge parallel to which the contact strip

DIMM module is in the range of 5.245 to 5.257 inches (133.22 to 133.52 mm) with a nominal dimension of 5.251 inches (133.37 mm), and that the overall height is in the range of 1.0 to 1.5 inches. Ex. 1003, 11, 13 (dimensions D1 and A, respectively); Ex. 1006, ¶¶ 96–98, 107–110.

2. Proposed Substitute Claim 9 and the Combination of Simpson and the Intel Specification

Petitioner opposes Patent Owner's Motion to Amend, arguing that proposed substitute claim 9 is unpatentable as obvious over Simpson and the Intel Specification. MTA Opp. 4–15.[8] Petitioner, with its Opposition to the Motion to Amend, submitted and relied upon additional declarations of Dr. Vivek Subramanian (Ex. 1016 and Ex. 1022). Patent Owner, in reply, argues that Simpson fails to disclose the "individually connected" limitation of claim 1 and that there was no motivation to utilize or modify Simpson's layout. MTA Reply 10–11.

Proposed substitute claim 9 is the combination of the limitations of independent claim 1, which define the printed circuit board configuration, with the addition of the circuit board width of dependent claim 8 and the addition of the circuit board height of dependent claim 4.

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runs is called the board width."); Ex. 1003, 11, 13 (Intel Specification Figure 1 depicting overall length dimension D1).

[8] Petitioner's Opposition also includes challenges based on the combination of Simpson and Karabatsos and the combination of Bechtolsheim, Tokunaga, and Karabatsos. Because we determine that the proposed substitute claim is unpatentable over the combination of Simpson and the Intel Specification, we do not reach the merits of Petitioner's arguments concerning these other combinations.

In articulating its opposition, Petitioner relies on Simpson for the general teaching of a layout of memory chips on a circuit board and relies on the Intel Specification for disclosing a "known design standard for the height and width" to which to apply Simpson's layout. MTA Opp. 5–6 (citing Ex. 1022 ¶¶ 17–18).

We have discussed the limitations of independent claim 1 above in the context of the challenge thereto in the Petition. The limitation of claim 8, now incorporated into proposed substitute claim 9, recites the "printed circuit board has a width of 5.25 inches." Dr. Subramanian testifies credibly that "[b]y mid-2001, the dimensions of printed circuit boards had been standardized for some time," and points to the Intel Specification's disclosure of the 5.25 inch dimension. Ex. 1006 ¶¶ 106–107; *see also* Ex. 1001, 4:53–55 (the '414 patent acknowledging that "[t]his board width [of 5.25 inches] has gained acceptance in the case of memory module boards."). We find that the claimed circuit board width was known in the art.

The limitation of claim 4, also now incorporated into proposed substitute claim 9, recites that the printed circuit board "has a height of 1 to 1.2 inches perpendicular to said contact strip." The claimed range falls completely within the range disclosed in the Intel Specification. "[A] prior art reference that discloses a range encompassing a somewhat narrower claimed range is sufficient to establish a *prima facie* case of obviousness." *In re Peterson*, 315 F.3d 1325, 1330 (Fed. Cir. 2003). Petitioner persuasively argues and presents evidentiary support that there was a recognized market need for

"low profile" memory modules, thus providing a reason for one of ordinary skill to target the claimed height range when designing a memory module. MTA Opp. 13–14 (citing Ex. 1016 ¶¶ 50–52, 56); *see* Ex. 1017 ¶¶ 27–28; Ex. 1006 ¶ 39; *id*. at ¶ 28 (the Karabatsos reference disclosing a "low profile DIMM" circuit board "having a height of approximately 1.2 inches, and a width of approximately 5.25 inches").

Patent Owner does not ascribe any criticality to the claimed height range and does not dispute that that range was known in the art. *See, e.g.*, MTA Reply 10–11; Prelim. Resp. 42 (Patent Owner: "While the Intel Specification may disclose that its memory module has a height of 1.0 to 1.2 inches, such a disclosure in a completely different system that requires surface mounted DRAM chips, not socketed DRAM chips, does not mean that a POSITA would be able to arrange two rows of sockets in Simpson to limit its height to 1.0 to 1.2 inches."); *but see* MTA 2 (Patent Owner arguing that the *combination* of component layout and height is absent in the prior art). Similarly, the '414 patent matter-of-factly states that "[t]he printed circuit board preferably has a height of 1 to 1.2 inches perpendicular to the contact strip," but does not state a basis for that preference. Ex. 1001, 4:7–8; *see also id*. at 6:50–56 (referring to the range in the same context as a standard DIMM design specification). Patent Owner, in the Motion to Amend, focuses on the layout of the circuit board while characterizing the height range merely as the result that flows from that layout. *See* MTA 2 ("The '414 Patent . . . recognize[es] and utilize[es] unique features relating to the placements of the

error correction chip and various passive elements on the Printed Circuit Board . . . [which] permitted the PCB height to be reduced to 1.0–1.2 inches . . . .").

We determine that Petitioner has provided an articulated reason with rational underpinning to support the conclusion of obviousness of subject matter having the recited width and height.

Petitioner, also relying on the testimony of Dr. Subramanian, demonstrates that an ordinary skilled artisan would have had a reasonable expectation of success. MTA Opp. 4–11 (citing Ex. 1006 ¶¶ 37–41; Ex. 1022 ¶¶ 17–30). Specifically, Petitioner persuasively shows that one of ordinary skill in the art would have been able to apply Simpson's chip layout on a circuit board having the claimed width and height dimensions. *Id.*[9]

In reply to Petitioner's opposition, Patent Owner argues that the "housing . . . being individually connected" limitation incorporated from claim 1 is missing from the combination of Simpson and the Intel Specification. MTA Reply 10–11. Patent Owner asserts that "Simpson's alleged memory chips are connected to sockets, that are in turn connected to

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[9] In reaching our determination, we do not rely on the Kiehl reference (Ex. 1020 (German application), Ex. 1021 (English translation)) or Dr. Subramanian's testimony pertaining thereto. Petitioner argues that "Kiehl provides clear evidence that memory chips existed contemporaneous to the '414 patent that would have permitted an arrangement of chips according to Simpson's pattern on a 5.25" by 1.2" PCB." MTA Surreply 7. However, Petitioner acknowledges that it is not alleging that Kiehl is prior art, merely "contemporaneous." *Id.* (asserting that certain applications were filed in Germany within two months of each other).

its printed circuit board," and thus, Simpson discloses an indirect connection. MTA Reply 10 (citing Ex. 1002, Fig. 1, 13:18-28). For the reasons set forth above in the discussion of claim construction, this argument is not persuasive, and we find that Simpson discloses memory housings individually connected to the circuit board.

Patent Owner also argues "[n]or was there motivation to utilize or modify Simpson's socketed invention as claimed." *Id.* at 11. Specifically, Patent Owner asserts that Simpson was concerned with an upgradable memory board and does not teach a reason for or benefit of the disclosed layout. *Id*. This argument is not persuasive. In an obviousness analysis, the prior art need not be directed to the same problem as the patentee and the references need not provide an explicit statement of motivation directed to the claimed subject matter. *See KSR Int'l. Co. v. Teleflex Inc.*, 550 U.S. 398, 418–20 (2007). Further, Patent Owner's argument, focusing only on the need discussed in Simpson, fails to address Petitioner's reasoning based on the ordinary artisan's recognition of a need to have shorter memory boards and recognition that Simpson's layout was one possible choice applicable to low profile circuit boards (*see* MTA Opp. 5–6, 11–14).

Accordingly, we determine based on a preponderance of the evidence that proposed substitute claim 9 is unpatentable, under 35 U.S.C. § 103(a), as obvious over Simpson and the Intel Specification. For this reason, Patent Owner's Motion to Amend is *denied*.

IV. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 5–8 of the '414 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Simpson.

Additionally, we determine, based on a preponderance of the evidence in the entire trial record, that proposed substitute claim 9 is unpatentable, under 35 U.S.C. § 103(a), as obvious over Simpson and the Intel Specification.

V. ORDER

For the foregoing reasons, it is

ORDERED that claims 1 and 5–8 of the '414 patent have been proven to be unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Amend is *denied*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

For PETITIONER:

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Martha Hopkins
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For PATENT OWNER:

Kenneth Weatherwax

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APPENDIX J

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE
PATENT TRIAL AND APPEAL BOARD

GENERAL ORDER IN CASES REMANDED UNDER A*RTHREX, INC. V. SMITH & NEPHEW, INC.*, 941 F.3D 1320 (FED. CIR. 2019)

GENERAL ORDER

Before SCOTT R. BOALICK, *Chief Administrative Patent Judge*.

BOALICK, *Chief Administrative Patent Judge*.

The United States Patent and Trademark Office ("Office") has received from the United States Court of Appeals for the Federal Circuit ("Federal Circuit") numerous Orders that rely on the Federal Circuit's decision in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019). Those Orders have already vacated more than 100 decisions by the Patent Trial and Appeal Board ("Board"), and more such Orders are expected. The Orders instruct the

Board to conduct further proceedings on remand before newly-designated Board panels.

Several parties in Board matters that have been subject to such Orders have informed the Office that they intend to seek review of the pertinent Order by the Supreme Court of the United States ("Supreme Court"). Meanwhile, in accordance with the Board's Standard Operating Procedure 9 ("SOP 9"), parties are contacting the Board to schedule teleconferences with the appropriate Board panel in their proceeding. To avoid burdening the Office and the parties until all appellate rights have been exhausted, I exercise my discretion to: (1) suspend the requirements in SOP 9 in cases remanded by the Federal Circuit under Arthrex; and (2) hold all such cases in administrative abeyance until the Supreme Court acts on a petition for certiorari or the time for filing such petitions expires.

ORDER

It is therefore ORDERED that the following matters are held in abeyance:

1. App. Ser. No. 95/001,679
2. App. Ser. No. 95/001,754
3. App. Ser. No. 95/001,792
4. App. Ser. No. 95/001,851
5. CBM2017-00064
6. CBM2017-00065
7. CBM2017-00066
8. CBM2017-00067
9. CBM2018-00034

10. IPR2014-01235
11. IPR2015-00249
12. IPR2015-01046
13. IPR2015-01047
14. IPR2016-00693
15. IPR2016-00957
16. IPR2016-01542
17. IPR2016-01621
18. IPR2016-01622
19. IPR2016-01756
20. IPR2017-01218
21. IPR2017-00058
22. IPR2017-00116
23. IPR2017-00198
24. IPR2017-00275
25. IPR2017-00350
26. IPR2017-00351
27. IPR2017-00352
28. IPR2017-00353
29. IPR2017-00524
30. IPR2017-00901
31. IPR2017-00950
32. IPR2017-00951
33. IPR2017-00952
34. IPR2017-01048

35. IPR2017-01049
36. IPR2017-01050
37. IPR2017-01256
38. IPR2017-01391
39. IPR2017-01392
40. IPR2017-01393
41. IPR2017-01405
42. IPR2017-01406
43. IPR2017-01409
44. IPR2017-01410
45. IPR2017-01500
46. IPR2017-01707
47. IPR2017-01714
48. IPR2017-01735
49. IPR2017-01736
50. IPR2017-01737
51. IPR2017-01797
52. IPR2017-01798
53. IPR2017-01799
54. IPR2017-01800
55. IPR2017-01801
56. IPR2017-01802
57. IPR2017-01919
58. IPR2017-02131
59. IPR2017-02132

60. IPR2017-02136
61. IPR2017-02138
62. IPR2017-02158
63. IPR2018-00522
64. IPR2018-00864
65. IPR2018-00044
66. IPR2018-00187
67. IPR2018-00200
68. IPR2018-00205
69. IPR2018-00206
70. IPR2018-00207
71. IPR2018-00208
72. IPR2018-00272
73. IPR2018-00312
74. IPR2018-00329
75. IPR2018-00333
76. IPR2018-00336
77. IPR2018-00338
78. IPR2018-00339
79. IPR2018-00342
80. IPR2018-00343
81. IPR2018-00369
82. IPR2018-00374
83. IPR2018-00375
84. IPR2018-00404

85. IPR2018-00458

86. IPR2018-00486

87. IPR2018-00529

88. IPR2018-00571

89. IPR2018-00599

90. IPR2018-00680

91. IPR2018-00870

92. IPR2018-00871

93. IPR2018-00872

94. IPR2018-00873

95. IPR2018-00874

96. IPR2018-00875

97. IPR2018-00998

98. IPR2018-00999

99. IPR2018-01000

100. IPR2018-01004

101. IPR2018-01005

102. IPR2018-01066

103. IPR2018-01205

It is further ORDERED that any other matters remanded by the Federal Circuit under *Arthrex* will be held in abeyance.

/s/ Scott R. Boalick
Scott R. Boalick
Chief Administrative Patent Judge

APPENDIX K

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED.,
Appellant,
v.
KINGSTON TECHNOLOGY COMPANY, INC.,
Appellee

UNITED STATES,
Intervenor

2018-1768

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2016-01621.

ON PETITIONS FOR PANEL REHEARING AND REHEARING EN BANC

Before PROST, *Chief Judge*, NEWMAN, LOURIE, DYK, MOORE, O'MALLEY, REYNA, WALLACH, TARANTO, CHEN, HUGHES, and STOLL, *Circuit Judges*.

PER CURIAM.

O R D E R

Appellant Polaris Innovations Limited and Appellee Kingston Technology Company, Inc. separately filed petitions for rehearing en banc. Intervenor United States also filed a combined petition for panel rehearing and rehearing en banc. The petitions were first referred as petitions for rehearing to the panel that heard the appeal, and thereafter the petitions for rehearing en banc were referred to the circuit judges who are in regular active service.

Upon consideration thereof,

IT IS ORDERED THAT:

The petitions for panel rehearing are denied.

The petitions for rehearing en banc are denied.

The mandate of the court will issue on April 9, 2020.

FOR THE COURT

April 2, 2020
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

APPENDIX L

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED.,
Appellant,
v.
KINGSTON TECHNOLOGY COMPANY, INC.,
Appellee

UNITED STATES,
Intervenor

2018-1831

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-00116.

ON PETITIONS FOR PANEL REHEARING AND REHEARING EN BANC

Before PROST, *Chief Judge*, NEWMAN, LOURIE, DYK, MOORE, O'MALLEY, REYNA, WALLACH, TARANTO, CHEN, HUGHES, and STOLL, *Circuit Judges*.

PER CURIAM.

O R D E R

Intervenor United States and Appellant Polaris Innovations Limited separately filed petitions for rehearing en banc. The petitions were first referred as petitions for rehearing to the panel that heard the appeal, and thereafter the petitions for rehearing en banc were referred to the circuit judges who are in regular active service.

Upon consideration thereof,

IT IS ORDERED THAT:

The petitions for panel rehearing are denied.

The petitions for rehearing en banc are denied.

The mandate of the court will issue on March 23, 2020.

FOR THE COURT

March 16, 2020
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

APPENDIX M

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED.,
Appellant,
v.
KINGSTON TECHNOLOGY COMPANY, INC.,
Appellee

ANDREI IANCU, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1202

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2016-01622.

ON PETITIONS FOR PANEL REHEARING AND REHEARING EN BANC

POLARIS INNOVATIONS LIMITED v. KINGSTON TECHNOLOGY COMPANY

Before PROST, *Chief Judge*, NEWMAN, MAYER[1], LOURIE, DYK, MOORE, O'MALLEY, REYNA, WALLACH, TARANTO, CHEN, HUGHES, and STOLL, *Circuit Judges*.

PER CURIAM.

O R D E R

Appellant Polaris Innovations Limited and Appellee Kingston Technology Company, Inc. separately filed petitions for rehearing en banc. Intervenor Andrei Iancu also filed a combined petition for panel rehearing and rehearing en banc. The petitions were referred to the panel that heard the appeal, and thereafter the petitions for rehearing en banc were referred to the circuit judges who are in regular active service.

Upon consideration thereof,

IT IS ORDERED THAT:

The petitions for panel rehearing are denied.

The petitions for rehearing en banc are denied.

The mandate of the court will issue on April 21, 2020.

FOR THE COURT

April 14, 2020
Date

/s/ Peter R. Marksteiner
Peter R. Marksteiner
Clerk of Court

[1] Circuit Judge Mayer participated only in the decision on the petition for panel rehearing.

APPENDIX N

1. U.S. Const. Art. II, § 2, Cl. 2 provides:

He shall have Power, by and with the Advice and Consent of the Senate, to make Treaties, provided two thirds of the Senators present concur; and he shall nominate, and by and with the Advice and Consent of the Senate, shall appoint Ambassadors, other public Minsters and Consuls, Judges of the supreme Court, and all other Officers of the United States, whose Appointments are not herein otherwise provided for, and which shall be established by Law: but the Congress may be Law vest the Appointment of such inferior Officers, as they think proper, in the President alone, in the Courts of Law, or in the Heads of Departments.

2. 5 U.S.C. 7513 provides:

Cause and procedure

(a) Under regulations prescribed by the Office of Personnel Management, an agency may take an action covered by this subchapter against an employee only for such cause as will promote the efficiency of the service.

(b) An employee against whom an action is proposed is entitled to—

> (1) at least 30 days' advance written notice, unless there is reasonable cause to believe the employee has committed a crime for which a sentence of imprisonment may be imposed, stating the specific reasons for the proposed action;

(2) a reasonable time, but not less than 7 days, to answer orally and in writing and to furnish affidavits and other documentary evidence in support of the answer;

(3) be represented by an attorney or other representative; and

(4) a written decision and the specific reasons therefor at the earliest practicable date.

(c) An agency may provide, by regulation, for a hearing which may be in lieu of or in addition to the opportunity to answer provided under subsection (b)(2) of this section.

(d) An employee against whom an action is taken under this section is entitled to appeal to the Merit Systems Protection Board under section 7701 of this title.

(e) Copies of the notice of proposed action, the answer of the employee when written, a summary thereof when made orally, the notice of decision and reasons therefor, and any order effecting an action covered by this subchapter, together with any supporting material, shall be maintained by the agency and shall be furnished to the Board upon its request and to the employee affected upon the employee's request.

3. 15 U.S.C. 1501 provides:

Establishment of Department; Secretary; seal

There shall be at the seat of government an executive department to be known as the Department of Commerce, and a Secretary of Commerce, who shall be the head thereof, who shall

be appointed by the President, by and with the advice and consent of the Senate, and whose term and tenure of office shall be like that of the heads of the other executive departments; and the provisions of title 4 of the Revised Statutes, including all amendments thereto, shall be applicable to said department. The said Secretary shall cause a seal of office to be made for the said department of such device as the President shall approve, and judicial notice shall be taken of the said seal.

4. 35 U.S.C. 1 provides:

Establishment

(a) ESTABLISHMENT.—The United States Patent and Trademark Office is established as an agency of the United States, within the Department of Commerce. In carrying out its functions, the United States Patent and Trademark Office shall be subject to the policy direction of the Secretary of Commerce, but otherwise shall retain responsibility for decisions regarding the management and administration of its operations and shall exercise independent control of its budget allocations and expenditures, personnel decisions and processes, procurements, and other administrative and management functions in accordance with this title and applicable provisions of law. Those operations designed to grant and issue patents and those operations which are designed to facilitate the registration of trademarks shall be treated as separate operating units within the Office.

(b) OFFICES.—The United States Patent and Trademark Office shall maintain its principal office

in the metropolitan Washington, D.C., area, for the service of process and papers and for the purpose of carrying out its functions. The United States Patent and Trademark Office shall be deemed, for purposes of venue in civil actions, to be a resident of the district in which its principal office is located, except where jurisdiction is otherwise provided by law. The United States Patent and Trademark Office may establish satellite offices in such other places in the United States as it considers necessary and appropriate in the conduct of its business.

(c) REFERENCE.—For purposes of this title, the United States Patent and Trademark Office shall also be referred to as the "Office" and the "Patent and Trademark Office".

5. 35 U.S.C. 2 provides:

Powers and duties

(a) IN GENERAL.—The United States Patent and Trademark Office, subject to the policy direction of the Secretary of Commerce—

> (1) shall be responsible for the granting and issuing of patents and the registration of trademarks; and
>
> (2) shall be responsible for disseminating to the public information with respect to patents and trademarks.
>
> (b) SPECIFIC POWERS.—The Office—
>
> (1) shall adopt and use a seal of the Office, which shall be judicially noticed and with which letters patent, certificates of trademark registrations, and papers issued by the Office

shall be authenticated;

(2) may establish regulations, not inconsistent with law, which—

(A) shall govern the conduct of proceedings in the Office;

(B) shall be made in accordance with section 553 of title 5;

(C) shall facilitate and expedite the processing of patent applications, particularly those which can be filed, stored, processed, searched, and retrieved electronically, subject to the provisions of section 122 relating to the confidential status of applications;

(D) may govern the recognition and conduct of agents, attorneys, or other persons representing applicants or other parties before the Office, and may require them, before being recognized as representatives of applicants or other persons, to show that they are of good moral character and reputation and are possessed of the necessary qualifications to render to applicants or other persons valuable service, advice, and assistance in the presentation or prosecution of their applications or other business before the Office;

(E) shall recognize the public interest in continuing to safeguard broad access to the United States patent system through the reduced fee structure for small entities under section 41(h)(1);

(F) provide for the development of a

performance-based process that includes quantitative and qualitative measures and standards for evaluating cost-effectiveness and is consistent with the principles of impartiality and competitiveness; and

(G) may, subject to any conditions prescribed by the Director and at the request of the patent applicant, provide for prioritization of examination of applications for products, processes, or technologies that are important to the national economy or national competitiveness without recovering the aggregate extra cost of providing such prioritization, notwithstanding section 41 or any other provision of law;

(3) may acquire, construct, purchase, lease, hold, manage, operate, improve, alter, and renovate any real, personal, or mixed property, or any interest therein, as it considers necessary to carry out its functions;

(4)(A) may make such purchases, contracts for the construction, maintenance, or management and operation of facilities, and contracts for supplies or services, without regard to the provisions of subtitle I and chapter 33 of title 40, division C (except sections 3302, 3501(b), 3509, 3906, 4710, and 4711) of subtitle I of title 41, and the McKinney-Vento Homeless Assistance Act (42 U.S.C. 11301 et seq.); and

(B) may enter into and perform such purchases and contracts for printing services, including the process of composition, platemaking, presswork, silk screen processes,

binding, microform, and the products of such processes, as it considers necessary to carry out the functions of the Office, without regard to sections 501 through 517 and 1101 through 1123 of title 44;

(5) may use, with their consent, services, equipment, personnel, and facilities of other departments, agencies, and instrumentalities of the Federal Government, on a reimbursable basis, and cooperate with such other departments, agencies, and instrumentalities in the establishment and use of services, equipment, and facilities of the Office;

(6) may, when the Director determines that it is practicable, efficient, and cost-effective to do so, use, with the consent of the United States and the agency, instrumentality, Patent and Trademark Office, or international organization concerned, the services, records, facilities, or personnel of any State or local government agency or instrumentality or foreign patent and trademark office or international organization to perform functions on its behalf;

(7) may retain and use all of its revenues and receipts, including revenues from the sale, lease, or disposal of any real, personal, or mixed property, or any interest therein, of the Office;

(8) shall advise the President, through the Secretary of Commerce, on national and certain international intellectual property policy issues;

(9) shall advise Federal departments and agencies on matters of intellectual property policy in the United States and intellectual

property protection in other countries;

(10) shall provide guidance, as appropriate, with respect to proposals by agencies to assist foreign governments and international intergovernmental organizations on matters of intellectual property protection;

(11) may conduct programs, studies, or exchanges of items or services regarding domestic and international intellectual property law and the effectiveness of intellectual property protection domestically and throughout the world, and the Office is authorized to expend funds to cover the subsistence expenses and travel-related expenses, including per diem, lodging costs, and transportation costs, of persons attending such programs who are not Federal employees;

(12)(A) shall advise the Secretary of Commerce on programs and studies relating to intellectual property policy that are conducted, or authorized to be conducted, cooperatively with foreign intellectual property offices and international intergovernmental organizations; and

(B) may conduct programs and studies described in subparagraph (A); and

(13)(A) in coordination with the Department of State, may conduct programs and studies cooperatively with foreign intellectual property offices and international intergovernmental organizations; and

(B) with the concurrence of the Secretary of

State, may authorize the transfer of not to exceed $100,000 in any year to the Department of State for the purpose of making special payments to international intergovernmental organizations for studies and programs for advancing international cooperation concerning patents, trademarks, and other matters.

(c) CLARIFICATION OF SPECIFIC POWERS.—(1) The special payments under subsection (b)(13)(B) shall be in addition to any other payments or contributions to international organizations described in subsection (b)(13)(B) and shall not be subject to any limitations imposed by law on the amounts of such other payments or contributions by the United States Government.

(2) Nothing in subsection (b) shall derogate from the duties of the Secretary of State or from the duties of the United States Trade Representative as set forth in section 141 of the Trade Act of 1974 (19 U.S.C. 2171).

(3) Nothing in subsection (b) shall derogate from the duties and functions of the Register of Copyrights or otherwise alter current authorities relating to copyright matters.

(4) In exercising the Director's powers under paragraphs (3) and (4)(A) of subsection (b), the Director shall consult with the Administrator of General Services.

(5) In exercising the Director's powers and duties under this section, the Director shall consult with the Register of Copyrights on all copyright and related matters.

(d) CONSTRUCTION.—Nothing in this section shall be construed to nullify, void, cancel, or interrupt any pending request-for-proposal let or contract issued by the General Services Administration for the specific purpose of relocating or leasing space to the United States Patent and Trademark Office.

6. 35 U.S.C. 3 provides:

Officers and employees

(a) UNDER SECRETARY AND DIRECTOR.—

(1) IN GENERAL.—The powers and duties of the United States Patent and Trademark Office shall be vested in an Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office (in this title referred to as the "Director"), who shall be a citizen of the United States and who shall be appointed by the President, by and with the advice and consent of the Senate. The Director shall be a person who has a professional background and experience in patent or trademark law.

(2) DUTIES.—

(A) IN GENERAL.—The Director shall be responsible for providing policy direction and management supervision for the Office and for the issuance of patents and the registration of trademarks. The Director shall perform these duties in a fair, impartial, and equitable manner.

(B) CONSULTING WITH THE PUBLIC

ADVISORY COMMITTEES.—The Director shall consult with the Patent Public Advisory Committee established in section 5 on a regular basis on matters relating to the patent operations of the Office, shall consult with the Trademark Public Advisory Committee established in section 5 on a regular basis on matters relating to the trademark operations of the Office, and shall consult with the respective Public Advisory Committee before submitting budgetary proposals to the Office of Management and Budget or changing or proposing to change patent or trademark user fees or patent or trademark regulations which are subject to the requirement to provide notice and opportunity for public comment under section 553 of title 5, as the case may be.

(3) OATH.—The Director shall, before taking office, take an oath to discharge faithfully the duties of the Office.

(4) REMOVAL.—The Director may be removed from office by the President. The President shall provide notification of any such removal to both Houses of Congress.

(b) OFFICERS AND EMPLOYEES OF THE OFFICE.—

(1) DEPUTY UNDER SECRETARY AND DEPUTY DIRECTOR.—The Secretary of Commerce, upon nomination by the Director, shall appoint a Deputy Under Secretary of Commerce for Intellectual Property and Deputy Director of the United States Patent and Trademark Office who shall be vested with the

authority to act in the capacity of the Director in the event of the absence or incapacity of the Director. The Deputy Director shall be a citizen of the United States who has a professional background and experience in patent or trademark law.

(2) COMMISSIONERS.—

(A) APPOINTMENT AND DUTIES.—The Secretary of Commerce shall appoint a Commissioner for Patents and a Commissioner for Trademarks, without regard to chapter 33, 51, or 53 of title 5. The Commissioner for Patents shall be a citizen of the United States with demonstrated management ability and professional background and experience in patent law and serve for a term of 5 years. The Commissioner for Trademarks shall be a citizen of the United States with demonstrated management ability and professional background and experience in trademark law and serve for a term of 5 years. The Commissioner for Patents and the Commissioner for Trademarks shall serve as the chief operating officers for the operations of the Office relating to patents and trademarks, respectively, and shall be responsible for the management and direction of all aspects of the activities of the Office that affect the administration of patent and trademark operations, respectively. The Secretary may reappoint a Commissioner to subsequent terms of 5 years as long as the performance of the Commissioner as set forth

in the performance agreement in subparagraph (B) is satisfactory.

(B) SALARY AND PERFORMANCE AGREEMENT. —The Commissioners shall be paid an annual rate of basic pay not to exceed the maximum rate of basic pay for the Senior Executive Service established under section 5382 of title 5, including any applicable locality-based comparability payment that may be authorized under section 5304(h)(2)(C) of title 5. The compensation of the Commissioners shall be considered, for purposes of section 207(c)(2)(A) of title 18, to be the equivalent of that described under clause (ii) of section 207(c)(2)(A) of title 18. In addition, the Commissioners may receive a bonus in an amount of up to, but not in excess of, 50 percent of the Commissioners' annual rate of basic pay, based upon an evaluation by the Secretary of Commerce, acting through the Director, of the Commissioners' performance as defined in an annual performance agreement between the Commissioners and the Secretary. The annual performance agreements shall incorporate measurable organization and individual goals in key operational areas as delineated in an annual performance plan agreed to by the Commissioners and the Secretary. Payment of a bonus under this subparagraph may be made to the Commissioners only to the extent that such payment does not cause the Commissioners' total aggregate compensation in a calendar year to equal or exceed the

amount of the salary of the Vice President under section 104 of title 3.

(C) REMOVAL.—The Commissioners may be removed from office by the Secretary for misconduct or nonsatisfactory performance under the performance agreement described in subparagraph (B), without regard to the provisions of title 5. The Secretary shall provide notification of any such removal to both Houses of Congress.

(3) OTHER OFFICERS AND EMPLOYEES.—The Director shall—

(A) appoint such officers, employees (including attorneys), and agents of the Office as the Director considers necessary to carry out the functions of the Office; and

(B) define the title, authority, and duties of such officers and employees and delegate to them such of the powers vested in the Office as the Director may determine.

The Office shall not be subject to any administratively or statutorily imposed limitation on positions or personnel, and no positions or personnel of the Office shall be taken into account for purposes of applying any such limitation.

(4) TRAINING OF EXAMINERS.—The Office shall submit to the Congress a proposal to provide an incentive program to retain as employees patent and trademark examiners of the primary examiner grade or higher who are eligible for retirement, for the sole purpose of

training patent and trademark examiners.

(5) NATIONAL SECURITY POSITIONS.—The Director, in consultation with the Director of the Office of Personnel Management, shall maintain a program for identifying national security positions and providing for appropriate security clearances, in order to maintain the secrecy of certain inventions, as described in section 181, and to prevent disclosure of sensitive and strategic information in the interest of national security.

(6) ADMINISTRATIVE PATENT JUDGES AND ADMINISTRATIVE TRADEMARK JUDGES.—The Director may fix the rate of basic pay for the administrative patent judges appointed pursuant to section 6 and the administrative trademark judges appointed pursuant to section 17 of the Trademark Act of 1946 (15 U.S.C. 1067) at not greater than the rate of basic pay payable for level III of the Executive Schedule under section 5314 of title 5. The payment of a rate of basic pay under this paragraph shall not be subject to the pay limitation under section 5306(e) or 5373 of title 5.

(c) CONTINUED APPLICABILITY OF TITLE 5.— Officers and employees of the Office shall be subject to the provisions of title 5, relating to Federal employees.

(d) ADOPTION OF EXISTING LABOR AGREEMENTS.—The Office shall adopt all labor agreements which are in effect, as of the day before the effective date of the Patent and Trademark Office Efficiency Act, with respect to such Office (as

then in effect).

(e) CARRYOVER OF PERSONNEL.—

(1) FROM PTO.—Effective as of the effective date of the Patent and Trademark Office Efficiency Act, all officers and employees of the Patent and Trademark Office on the day before such effective date shall become officers and employees of the Office, without a break in service.

(2) OTHER PERSONNEL.—Any individual who, on the day before the effective date of the Patent and Trademark Office Efficiency Act, is an officer or employee of the Department of Commerce (other than an officer or employee under paragraph (1)) shall be transferred to the Office, as necessary to carry out the purposes of that Act, if—

(A) such individual serves in a position for which a major function is the performance of work reimbursed by the Patent and Trademark Office, as determined by the Secretary of Commerce;

(B) such individual serves in a position that performed work in support of the Patent and Trademark Office during at least half of the incumbent's work time, as determined by the Secretary of Commerce; or

(C) such transfer would be in the interest of the Office, as determined by the Secretary of Commerce in consultation with the Director.

Any transfer under this paragraph shall be effective as of the same effective date as

referred to in paragraph (1), and shall be made without a break in service.

(f) TRANSITION PROVISIONS.—

(1) INTERIM APPOINTMENT OF DIRECTOR.—On or after the effective date of the Patent and Trademark Office Efficiency Act, the President shall appoint an individual to serve as the Director until the date on which a Director qualifies under subsection (a). The President shall not make more than one such appointment under this subsection.

(2) CONTINUATION IN OFFICE OF CERTAIN OFFICERS.—(A) The individual serving as the Assistant Commissioner for Patents on the day before the effective date of the Patent and Trademark Office Efficiency Act may serve as the Commissioner for Patents until the date on which a Commissioner for Patents is appointed under subsection (b).

(B) The individual serving as the Assistant Commissioner for Trademarks on the day before the effective date of the Patent and Trademark Office Efficiency Act may serve as the Commissioner for Trademarks until the date on which a Commissioner for Trademarks is appointed under subsection (b).

7. 35 U.S.C. 6 provides:

Patent Trial and Appeal Board

(a) IN GENERAL.—There shall be in the Office a Patent Trial and Appeal Board. The Director, the Deputy Director, the Commissioner for Patents, the

Commissioner for Trademarks, and the administrative patent judges shall constitute the Patent Trial and Appeal Board. The administrative patent judges shall be persons of competent legal knowledge and scientific ability who are appointed by the Secretary, in consultation with the Director. Any reference in any Federal law, Executive order, rule, regulation, or delegation of authority, or any document of or pertaining to the Board of Patent Appeals and Interferences is deemed to refer to the Patent Trial and Appeal Board.

(b) DUTIES.—The Patent Trial and Appeal Board shall—

(1) on written appeal of an applicant, review adverse decisions of examiners upon applications for patents pursuant to section 134(a);

(2) review appeals of reexaminations pursuant to section 134(b);

(3) conduct derivation proceedings pursuant to section 135; and

(4) conduct inter partes reviews and post-grant reviews pursuant to chapters 31 and 32.

(c) 3-MEMBER PANELS.—Each appeal, derivation proceeding, post-grant review, and inter partes review shall be heard by at least 3 members of the Patent Trial and Appeal Board, who shall be designated by the Director. Only the Patent Trial and Appeal Board may grant rehearings.

(d) TREATMENT OF PRIOR APPOINTMENTS.—The Secretary of Commerce may, in the Secretary's discretion, deem the appointment of an administrative patent judge who,

before the date of the enactment of this subsection, held office pursuant to an appointment by the Director to take effect on the date on which the Director initially appointed the administrative patent judge. It shall be a defense to a challenge to the appointment of an administrative patent judge on the basis of the judge's having been originally appointed by the Director that the administrative patent judge so appointed was acting as a de facto officer.

8. 35 U.S.C. 141 provides:

Appeal to Court of Appeals for the Federal Circuit

(a) Examinations. An applicant who is dissatisfied with the final decision in an appeal to the Patent Trial and Appeal Board under section 134(a) may appeal the Board's decision to the United States Court of Appeals for the Federal Circuit. By filing such an appeal, the applicant waives his or her right to proceed under section 145.

(b) Reexaminations. A patent owner who is dissatisfied with the final decision in an appeal of a reexamination to the Patent Trial and Appeal Board under section 134(b) may appeal the Board's decision only to the United States Court of Appeals for the Federal Circuit.

(c) Post-grant and inter partes reviews. A party to an inter partes review or a post-grant review who is dissatisfied with the final written decision of the Patent Trial and Appeal Board under section 318(a) or 328(a) (as the case may be) may appeal the Board's decision only to the United States Court of

Appeals for the Federal Circuit.

(d) Derivation proceedings. A party to a derivation proceeding who is dissatisfied with the final decision of the Patent Trial and Appeal Board in the proceeding may appeal the decision to the United States Court of Appeals for the Federal Circuit, but such appeal shall be dismissed if any adverse party to such derivation proceeding, within 20 days after the appellant has filed notice of appeal in accordance with section 142, files notice with the Director that the party elects to have all further proceedings conducted as provided in section 146. If the appellant does not, within 30 days after the filing of such notice by the adverse party, file a civil action under section 146, the Board's decision shall govern the further proceedings in the case.

9. 35 U.S.C. 143 provides:

Proceedings on appeal

With respect to an appeal described in section 142, the Director shall transmit to the United States Court of Appeals for the Federal Circuit a certified list of the documents comprising the record in the Patent and Trademark Office. The court may request that the Director forward the original or certified copies of such documents during pendency of the appeal. In an ex parte case, the Director shall submit to the court in writing the grounds for the decision of the Patent and Trademark Office, addressing all of the issues raised in the appeal. The Director shall have the right to intervene in an appeal from a decision entered by the Patent Trial and Appeal Board in a derivation proceeding under section 135 or in an inter partes or post-grant review

under chapter 31 or 32. The court shall, before hearing an appeal, give notice of the time and place of the hearing to the Director and the parties in the appeal.

10. 35 U.S.C. 314 provides:

Institution of inter partes review

(a) THRESHOLD.—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

(b) TIMING.—The Director shall determine whether to institute an inter partes review under this chapter pursuant to a petition filed under section 311 within 3 months after—

(1) receiving a preliminary response to the petition under section 313; or

(2) if no such preliminary response is filed, the last date on which such response may be filed.

(c) NOTICE.—The Director shall notify the petitioner and patent owner, in writing, of the Director's determination under subsection (a), and shall make such notice available to the public as soon as is practicable. Such notice shall include the date on which the review shall commence.

(d) NO APPEAL.—The determination by the

Director whether to institute an inter partes review under this section shall be final and nonappealable.

11. 35 U.S.C. 316 provides:

Conduct of inter partes review

(a) REGULATIONS.—The Director shall prescribe regulations—

(1) providing that the file of any proceeding under this chapter shall be made available to the public, except that any petition or document filed with the intent that it be sealed shall, if accompanied by a motion to seal, be treated as sealed pending the outcome of the ruling on the motion;

(2) setting forth the standards for the showing of sufficient grounds to institute a review under section 314(a);

(3) establishing procedures for the submission of supplemental information after the petition is filed;

(4) establishing and governing inter partes review under this chapter and the relationship of such review to other proceedings under this title;

(5) setting forth standards and procedures for discovery of relevant evidence, including that such discovery shall be limited to—

(A) the deposition of witnesses submitting affidavits or declarations; and

(B) what is otherwise necessary in the interest of justice;

(6) prescribing sanctions for abuse of discovery, abuse of process, or any other improper use of the proceeding, such as to harass or to cause unnecessary delay or an unnecessary increase in the cost of the proceeding;

(7) providing for protective orders governing the exchange and submission of confidential information;

(8) providing for the filing by the patent owner of a response to the petition under section 313 after an inter partes review has been instituted, and requiring that the patent owner file with such response, through affidavits or declarations, any additional factual evidence and expert opinions on which the patent owner relies in support of the response;

(9) setting forth standards and procedures for allowing the patent owner to move to amend the patent under subsection (d) to cancel a challenged claim or propose a reasonable number of substitute claims, and ensuring that any information submitted by the patent owner in support of any amendment entered under subsection (d) is made available to the public as part of the prosecution history of the patent;

(10) providing either party with the right to an oral hearing as part of the proceeding;

(11) requiring that the final determination in an inter partes review be issued not later than 1 year after the date on which the Director notices the institution of a review under this chapter, except that the Director may, for good cause shown, extend the 1-year period by not more

than 6 months, and may adjust the time periods in this paragraph in the case of joinder under section 315(c);

(12) setting a time period for requesting joinder under section 315(c); and

(13) providing the petitioner with at least 1 opportunity to file written comments within a time period established by the Director.

(b) CONSIDERATIONS.—In prescribing regulations under this section, the Director shall consider the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under this chapter.

(c) PATENT TRIAL AND APPEAL BOARD.—The Patent Trial and Appeal Board shall, in accordance with section 6, conduct each inter partes review instituted under this chapter.

(d) AMENDMENT OF THE PATENT.—

(1) IN GENERAL.—During an inter partes review instituted under this chapter, the patent owner may file 1 motion to amend the patent in 1 or more of the following ways:

(A) Cancel any challenged patent claim.

(B) For each challenged claim, propose a reasonable number of substitute claims.

(2) ADDITIONAL MOTIONS.—Additional motions to amend may be permitted upon the joint request of the petitioner and the patent owner to materially advance the settlement of a

proceeding under section 317, or as permitted by regulations prescribed by the Director.

(3) SCOPE OF CLAIMS.—An amendment under this subsection may not enlarge the scope of the claims of the patent or introduce new matter.

(e) EVIDENTIARY STANDARDS.—In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.

12. 35 U.S.C. 318 provides:

Decision of the Board

(a) FINAL WRITTEN DECISION.—If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d).

(b) CERTIFICATE.—If the Patent Trial and Appeal Board issues a final written decision under subsection (a) and the time for appeal has expired or any appeal has terminated, the Director shall issue and publish a certificate canceling any claim of the patent finally determined to be unpatentable, confirming any claim of the patent determined to be patentable, and incorporating in the patent by operation of the certificate any new or amended claim determined to be patentable.

(c) INTERVENING RIGHTS.—Any proposed

amended or new claim determined to be patentable and incorporated into a patent following an inter partes review under this chapter shall have the same effect as that specified in section 252 for reissued patents on the right of any person who made, purchased, or used within the United States, or imported into the United States, anything patented by such proposed amended or new claim, or who made substantial preparation therefor, before the issuance of a certificate under subsection (b).

(d) DATA ON LENGTH OF REVIEW.—The Office shall make available to the public data describing the length of time between the institution of, and the issuance of a final written decision under subsection (a) for, each inter partes review.

13. 35 U.S.C. 319 provides:

Appeal

A party dissatisfied with the final written decision of the Patent Trial and Appeal Board under section 318(a) may appeal the decision pursuant to sections 141 through 144. Any party to the inter partes review shall have the right to be a party to the appeal.